PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2003-188727

(43)Date of publication of application : 04.07.2003

(51)Int.Cl. H03M 1/44

(21)Application number : 2001-384369

(22)Date of filing : 18.12.2001

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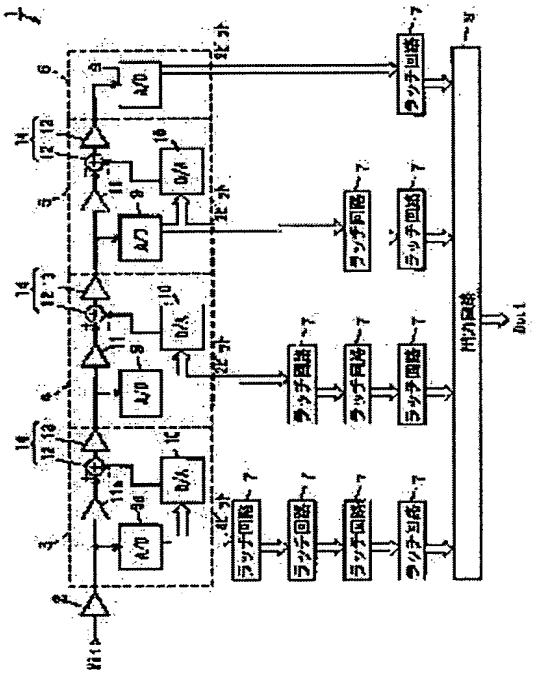
(54) ANALOG/DIGITAL CONVERTER CIRCUIT

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a pipeline type analog/digital (A/D) converter circuit in which a change in the voltage range of an analog input signal or change of an input system between a differential double end input and a single end input can be easily performed without redesigning a circuit configuration.

SOLUTION: When the voltage range of the analog input signal is VINp-p, the full scale range of a sub A/D converter 9 is switched to VINp-p, and the gain of an operational amplifier circuit 11a is switched into single. When the voltage range of the analog input signal is VINp-p/2, the full scale range of the sub A/D converter 9 is switched to VINp-p/2 and the gain of the operational amplifier circuit 11a is switched into double.



* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1]An analog-to-digital circuit comprising:
An analog-digital converter which has the multi stage pipeline constitution which consists of two or more steps of circuits and from which a circuit of each stage except a circuit of a final stage changes an inputted analog signal into a digital signal.
A digital-to-analog converter which changes into an analog signal a digital signal outputted from said analog-digital converter.
Have the 1st arithmetic amplifier that amplifies difference of an analog signal inputted and an analog signal outputted from said digital-to-analog converter, and a circuit of a final stage, An analog-digital converter which changes an inputted analog signal into a digital signal is included, An analog-digital converter which has a switching means from which at least one step of circuit except a circuit of a final stage changes a full-scale range to two or more steps, At least one of the 1st arithmetic amplifiers that have a switching means which changes a digital-to-analog converter and a profit which have a switching means which changes a full-scale range to two or more steps to two or more steps is included, And/or, an analog-digital converter which has a switching means from which a circuit of a final stage changes a full-scale range to two or more steps.

[Claim 2]A circuit of each stage except a circuit of a final stage includes further the 2nd arithmetic amplifier that amplifies an inputted analog signal and is given to said 1st arithmetic amplifier, The analog-to-digital circuit according to claim 1, wherein said 2nd arithmetic amplifier of at least one step of circuit except a circuit of a final stage has a switching means which changes a profit to two or more steps.
[Claim 3]The analog-to-digital circuit according to claim 1 or 2, wherein said 1st arithmetic amplifier of at least one step of circuit except a circuit of a final stage has a switching means which changes a profit to two or more steps.
[Claim 4]The analog-to-digital circuit according to any one of claims 1 to 3, wherein said analog-digital converter of at least one step of circuit has a switching means which changes a full-scale range to two or more steps.
[Claim 5]The analog-to-digital circuit according to any one of claims 1 to 4, wherein said digital-to-analog converter of at least one step of circuit except a circuit of a final stage has a switching means which changes a full-scale range to two or more steps.
[Claim 6]Said 2nd arithmetic amplifier of at least one step of said circuit, On a profit which becomes settled with a value of said input capacitance, and a value of said feedback capacity, have input capacitance, feedback capacity, and an operational amplifier, amplify an inputted analog signal, and said switching means, The analog-to-digital circuit according to claim 2 containing a variable region which sets either [at least] a value of said input capacitance, or a value of said feedback capacity as variable.
[Claim 7]The analog-to-digital circuit according to claim 6, wherein said variable region contains a switch part changed to a state or the state where it connected too hastily where a part of said input capacitance or said feedback capacity was separated.

[Claim 8]Said 1st arithmetic amplifier of at least one step of said circuit, On a profit which becomes settled with a value of said input capacitance, and a value of said feedback capacity, have input capacitance, feedback capacity, and an operational amplifier, amplify an inputted analog signal, and said switching means, The analog-to-digital circuit according to claim 3 containing a variable region which sets either [at least] a value of said input capacitance, or a value of said feedback capacity as variable.
[Claim 9]The analog-to-digital circuit according to claim 8, wherein said variable region contains a switch part changed to a state or the state where it connected too hastily where a part of said input capacitance or said feedback capacity was separated.
[Claim 10]The analog-to-digital circuit according to claim 9 characterized by connecting said switch part to said 2nd capacity in series or in parallel including the 1st and 2nd capacity by which said feedback capacity was provided in parallel or in series between an input terminal of said operational amplifier, and an output terminal.
[Claim 11]The analog-to-digital circuit according to claim 10, wherein said switch part is connected to an output terminal of said operational amplifier.
[Claim 12]The analog-to-digital circuit according to claim 9 characterized by connecting said switch part to said 2nd capacity in series or in parallel including the 1st and 2nd capacity by which said input capacitance was provided in an input terminal of said operational amplifier in parallel or in series.
[Claim 13]The analog-to-digital circuit according to claim 12 connecting to an input side of said 2nd capacity before said switch part.
[Claim 14]The analog-to-digital circuit comprising according to claim 4:
Circuit generating reference voltage where said analog-digital converter of at least one step of circuit generates two or more reference voltage.
A variable region which sets as variable two or more reference voltage in which said switching means is generated by said circuit generating reference voltage including two or more comparators compared with an analog signal into which two or more reference voltage generated by said circuit generating reference voltage was inputted.

[Claim 15]The analog-to-digital circuit comprising according to claim 5:
Circuit generating reference voltage where said digital-to-analog converter of at least one step of circuit except a circuit of a final stage generates reference voltage.
Two or more capacity connected to a common terminal.
Two or more switches which give reference voltage which was connected between said circuit generating reference voltage and said two or more capacity, and was generated by said circuit generating reference voltage according to a digital signal inputted to said two or more capacity, respectively are included, A variable region which sets as variable reference voltage in which said switching means is generated by said circuit generating reference voltage.

[Translation done.]

the full-scale range of sub A/D converter 9] $_{p-p}$ twice many / 4 in order to take consistency with the output voltage range of the arithmetic amplifier 11 which has the profit 2.
[0010]Next, operation of the analog-to-digital circuit 1 of drawing 23 is explained. The sample hold circuit 2 samples the analog input signal Vin, and carries out fixed time maintenance. The analog input signal Vin outputted from the sample hold circuit 2 is transmitted to the 1st step of circuit 3.
[0011]In the 1st step of circuit 3, sub A/D converter 9 performs an analog to digital to the analog input signal Vin of voltage range VIN_{p-p}. Here, the full-scale range of sub A/D converter 9 is VIN_{p-p} as mentioned above. The digital output (2^9, 2^8, 2^7, 2^6) which is an analog-to-digital result of sub A/D converter 9 is transmitted to the output circuit 8 via the four latch circuitry 7 while it is transmitted to D/A converter 10. The normal output voltage range of D/A converter 10 is expressed like a following formula.
[0012]
(The 1st step of resolution-1) x(full-scale range of D/A converter 10)/(the 1st step of resolution)
= $(2^4-1) \times (VIN_{p-p}) / 2^4 = 15VIN_{p-p}/16$ one side and the arithmetic amplifier 11 sample the analog input signal Vin, and amplify and hold it. The output voltage range of the arithmetic amplifier 11 is expressed like a following formula.
[0013]
(Voltage range VIN_{p-p} of the analog input signal Vin) x (profit of the arithmetic amplifier 11)
= The $VIN_{p-p} \times 1 = VIN_{p-p}$ subtraction amplifier 14 subtracts and amplifies the analog input signal Vin and the D/A conversion result of D/A converter 10 which were outputted from the arithmetic amplifier 11. The output of the subtraction amplification width circuit 14 is transmitted to the 2nd step of circuit 4. The output voltage range of the 1st step of subtraction amplifier 14 is expressed like a following formula.
[0014]
(Output voltage range of the arithmetic amplifier 11) x (- (normal output voltage range of D/A converter 10)) (profit of the subtraction amplifier 14)
= (VIN_{p-p}) (- $(15VIN_{p-p}/16)$) In the x2 $= VIN_{p-p}/82$ step circuit 4, sub A/D converter 9 performs an A/D conversion to the output of the subtraction amplifier 14 of the 1st step of circuit 3. The A/D conversion result of sub A/D converter 9 is transmitted to the output circuit 8 via the three latch circuitry 7 while it is transmitted to D/A converter 10.Thereby, a 2-bit digital output (2^5, 2^4) is obtained at least for Nakagami from the 2nd step of circuit 4. The normal output voltage range of D/A converter 10 is expressed like a following formula.
[0015]
(The 2nd step of resolution-1) x(full-scale range of D/A converter 10)/(the 2nd step of resolution)
= $(2^2-1) \times (VIN_{p-p}/4) / 2^2 = 3VIN_{p-p}/16$ one side and the arithmetic amplifier 11 amplify the output of the arithmetic amplifier 13 of the 1st step of circuit 3. The output voltage range of the arithmetic amplifier 11 is expressed like a following formula.
[0016]
(Output voltage range of the 1st step of subtraction amplifier 14) x (profit of the arithmetic amplifier 11)
= $(VIN_{p-p}/8)$ The x2 $= VIN_{p-p}/4$ subtraction amplifier 14 subtracts and amplifies the output of the arithmetic amplifier 11, and the D/A conversion result of D/A converter 10. The output of the subtraction amplifier 14 is transmitted to the 3rd step of circuit 5. The range of the output voltage of the 2nd step of subtraction amplifier 14 is expressed like a following formula.
[0017]
(Output voltage range of the arithmetic amplifier 11) x (- (normal output voltage range of D/A converter 10)) (profit of the subtraction amplifier 14)

= (VIN_{p-p}/4) (- (3VIN_{p-p}/16)) In the x2 =VIN_{p-p}/83 step circuit 5, the same operation as the 2nd step of circuit 4 is performed to the output of the subtraction amplifier 14 of the 2nd step of circuit 3. Thereby, a 2-bit digital output (2^3, 2^2) is obtained at least for Nakashita from the 3rd step of circuit 5. The output voltage range of each part is the same as that of the 2nd step of circuit 4.

[0018]In the 4th step of circuit 6, sub A/D converter 9 performs an A/D conversion to the output of the subtraction amplifier 14 of the 3rd step of circuit 5, and the digital output (2^1, 2^0) of 2 bits of low ranks is obtained.

[0019]The digital output of the 1st step - the 4th step of circuits 3-6 arrives at the output circuit 8 simultaneously through each latch circuitry 7. That is, each latch circuitry 7 is formed in order to take the synchronization of the digital output of each circuits 3-6.

[0020]The output circuit 8 carries out the after [a digital compensation process] parallel output of the 10-bit digital output Dout of the analog input signal Vin, when required.

[0021]Thus, even if the conversion number of bits increases and LSB (Least Significant Bit) becomes small with reduction in power supply voltage, the resolution of sub A/D converter 9 can be raised and sufficient conversion precision is acquired.

[0022]Drawing 24 (a) is a figure for the circuit diagram and drawing 24 (b) in which the composition of the subtraction amplifier of the analog-to-digital circuit of drawing 23 is shown to explain operation of the subtraction amplifier of drawing 24 (a).

[0023]In drawing 24, the inversed input terminal of the operational amplifier 101 is connected to the node nb, and the non-inversed input terminal is grounded. The output terminal of the operational amplifier 101 is connected to the inversed input terminal via the capacitor 102 while being connected to the node no. Switch SW1 is connected between the inversed input terminal of the operational amplifier 1, and a non-inversed input terminal, and the capacitor 103 is connected between the node nb and the node na. It is connected to the node n1 via switch SW2, and the node na is connected to the node n2 via switch SW3. These switch SW2 and SW3 are constituted by the CMOS switch which usually consists of a CMOS (complementary-type metal oxide semiconductor) field effect transistor.

[0024]Voltage V_1 is inputted into the node n1, voltage V_2 is inputted into the node n2, and voltage V_O is outputted from the node no.

[0025]Here, operation of the subtraction amplifier of drawing 24 (a) is explained, referring to drawing 24 (b). Capacity value of the capacitor 101 is set to C, capacity value of the capacitor 103 is set to KC, and earth potentials are made into V_G. K is a constant.

[0026]First, switch SW1 and switch SW2 are made one, and switch SW3 is turned OFF. Thereby, the voltage of the node na serves as V_1. The voltage of the node no is set to 0. At this time, the electric charge Qa of the node nb becomes like a following formula.

[0027]After turning OFF $Qa=(V_G-V_1)$ KC, next switch SW1, switch SW2 is turned OFF and switch SW3 is made one. Thereby, the voltage of the node na serves as V_2. The voltage of the node no serves as V_O. In order to carry out the imaginary earth of the node nb at this time, the electric charge Qb of the node nb becomes like a following formula.

[0028]

Since there is no course out of which an electric charge escapes from and comes in the $Qb=(V_G-V_2)$ $KC+(V_G-V_O)$ C node nb, it becomes Qa=Qb with conservation of charge. Therefore, a following formula is materialized.

[0029](V_G-V_1) Voltage V_O of a $KC=(V_G-V_2)$ $KC+(V_G-V_O)$ C top type to the node no becomes like a following formula.

[0030]Voltage V_2 is subtracted from $V_O=V_G+(V_1-V_2)$ K, thus voltage V_1, and the subtraction value is amplified K times.

[0031]Therefore, a subtraction amplifier has a function which outputs the difference of voltage

V_1 and voltage V_2 by the profit decided by the capacity factor of the capacitor 103 and the capacitor 102. For example, a sample hold function 1 time the profit of this will be given to a subtraction amplifier by setting it as KC=C (K= 1).

[0032]Drawing 25 is a figure showing the composition of the sub A/D converter used in the analog-to-digital circuit of drawing 23.

[0033]Two or more comparators 900 are arranged in the parallel connected type analog-digital converter 9 of drawing 25. The analog input voltage Vin is given to one input terminal of two or more comparators 900, and the reference voltage obtained by carrying out the partial pressure of the voltage between the high potential side reference voltage VRT and the low voltage side reference voltage VRB to the input terminal of another side by two or more resistance R is given, respectively. Each comparator 900 compares the voltage of one input terminal with the voltage of the input terminal of another side. The digital code Dcode can be obtained by encoding the comparison result of two or more comparators 900 with the encoder 910.

[0034]By the way, when the voltage range of the analog input signal given to an analog-to-digital circuit is changed, Or to change the method of the analog input signal given to an analog-to-digital circuit in a differential double end input and a single-ended input, it is necessary to change the specification of an analog-to-digital circuit.

[0035]Here, a differential double end input and a single-ended input are explained. Drawing 26 (a) and (b) is a figure for explaining the analog to digital in a differential double end input and a single-ended input. A horizontal axis shows the analog input voltage VIN, and a vertical axis shows the outputted digital code Dcode.

[0036]As shown in drawing 26 (a), at the time of a differential double end input, the right side analog input voltage Vin (+) and the negative side analog input voltage Vin (-) of the analog input signal Vin change complementarily. Thereby, the difference of the right side analog input voltage Vin (+) and the negative side analog input voltage Vin (-) serves as voltage range VIN_{p-p} of the analog input signal Vin.

[0037]Therefore, as shown in drawing 26 (a), the right side analog input voltage Vin (+) changes from 1.0V in 2.0, When the negative side analog input voltage Vin (-) changes in 2.0V to 1.0V, the voltage range of the analog input signal Vin is set to 2.0V from the operation of Vin(+)-Vin (-).

[0038]On the other hand, as shown in drawing 26 (b), at the time of a single-ended input, the right side analog input voltage Vin (+) changes. Thereby, the voltage range of the right side analog input voltage Vin (+) turns into a voltage range of the analog input signal Vin.

[0039]Therefore, as shown in drawing 26 (b), when the right side analog input voltage Vin (+) changes in 1.0V to 2.0V, the voltage range of an analog input signal is set to 1.0V.

[0040]That is, if the voltage range of the analog input signal Vin of a differential double end input method is made into $2VIN_{p-p}$, the voltage range of the analog input signal Vin of a single-ended input method will serve as VIN_{p-p}.

[0041]Thus, with a differential double end input method and a single-ended input method, even if the range of change of each analog input voltage is the same, the voltage ranges of an analog input signal will differ.

[0042]In the above-mentioned conventional analog-to-digital circuit, when changing the voltage range of an analog input signal, or when changing the input method of an analog input signal, it is necessary to redesign circuitry.

[0043]The purpose of this invention is to provide the pipeline type analog-to-digital circuit which can change the input method between change of the voltage range of an analog input signal or a differential double end input, and a single-ended input easily without redesigning circuitry.

[0044]

[The means for solving a technical problem and an effect of the invention] (1) The analog-to-digital circuit concerning the 1st invention invention of the 1st, Have the multi stage pipeline constitution which consists of two or more steps of circuits, and the circuit of each stage except the circuit of a final stage, The analog-digital converter which changes the inputted analog signal into a digital signal, The digital-to-analog converter which changes into an analog

signal the digital signal outputted from an analog-digital converter, Have the 1st arithmetic amplifier that amplifies the difference of the analog signal inputted and the analog signal outputted from a digital-to-analog converter, and the circuit of a final stage, The analog-digital converter which changes the inputted analog signal into a digital signal is included, The analog-digital converter which has a switching means from which at least one step of circuit except the circuit of a final stage changes a full-scale range to two or more steps, At least one of the 1st arithmetic amplifiers that have a switching means which changes the digital-to-analog converter and profit which have a switching means which changes a full-scale range to two or more steps to two or more steps is included, And/or, the circuit of a final stage contains the analog-digital converter which has a switching means which changes a full-scale range to two or more steps.
[0045]In an analog-to-digital circuit concerning this invention, An analog-digital converter which has a switching means from which at least one step of circuit except a circuit of a final stage changes a full-scale range to two or more steps, At least one of the 1st arithmetic amplifiers that have a switching means which changes a digital-to-analog converter and a profit which have a switching means which changes a full-scale range to two or more steps, and to change to two or more steps is included, And/or, since a circuit of a final stage contains an analog-digital converter which has a switching means which changes a full-scale range to two or more steps, At least one of a full-scale range of an analog-to-digital circuit, a full-scale range of a digital-to-analog converter, and profits of the 1st arithmetic amplifier can be changed.
[0046]Redesign of circuitry becomes unnecessary even if a voltage range of an analog input signal is changed by that cause by changing a differential double end input method into a single-ended input method. Redesign of circuitry becomes unnecessary, when changing a voltage range of an analog input signal of a single-ended input, or also when changing a voltage range of an analog input signal of a differential double end input.
[0047]Therefore, an input method between change of a voltage range of an analog input signal or a differential double end input, and a single-ended input can be changed easily, without redesigning circuitry.
[0048]As a result, while being able to attain shortening of a development cycle of an analog-to-digital circuit, low power consumption can be easily performed by optimizing optimization of a voltage range.
[0049](2) An analog-to-digital circuit concerning the 2nd invention invention of the 2nd, In composition of an analog-to-digital circuit concerning the 1st invention, a circuit of each stage except a circuit of a final stage, The 2nd arithmetic amplifier of at least one step of circuit except a circuit of a final stage has a switching means which changes a profit to two or more steps, including further the 2nd arithmetic amplifier that amplifies an inputted analog signal and is given to the 1st arithmetic amplifier.
[0050]In this case, by changing a profit of the 2nd arithmetic amplifier of at least one step of circuit to two or more steps, It becomes possible to change an input method between change of a voltage range of an analog input signal or a differential double end input, and a single-ended input easily, without redesigning circuitry.
[0051](3) In composition of an analog-to-digital circuit which an analog-to-digital circuit concerning the 3rd invention invention of the 3rd requires for the 1st or 2nd invention, the 1st arithmetic amplifier of at least one step of circuit except a circuit of a final stage has a switching means which changes a profit to two or more steps.
[0052]In this case, by changing a profit of the 1st arithmetic amplifier of at least one step of circuit to two or more steps, It becomes possible to change an input method between change of a voltage range of an analog input signal or a differential double end input, and a single-ended input easily, without redesigning circuitry.
[0053](4) An analog-to-digital circuit concerning the 4th invention invention of the 4th, In composition of an analog-to-digital circuit concerning the 1st - the 3rd one of inventions, an analog-digital converter of at least one step of circuit has a switching means which changes a full-scale range to two or more steps.
[0054]In this case, a full-scale range of an analog-digital converter of at least one step of circuit to two or more steps by switchable ******. It becomes possible to change an input method

between change of a voltage range of an analog input signal or a differential double end input, and a single-ended input easily, without redesigning circuitry.
[0055](5) An analog-to-digital circuit concerning the 5th invention invention of the 5th, In composition of an analog-to-digital circuit concerning the 1st - the 4th one of inventions, a digital-to-analog converter of at least one step of circuit except a circuit of a final stage has a switching means which changes a full-scale range to two or more steps.
[0056]In this case, by changing a full-scale range of a digital-to-analog converter of at least one step of circuit to two or more steps, It becomes possible to change an input method between change of a voltage range of an analog input signal or a differential double end input, and a single-ended input easily, without redesigning circuitry.
[0057](6) An analog-to-digital circuit concerning the 6th invention invention of the 6th, In composition of an analog-to-digital circuit concerning the 2nd invention, the 2nd arithmetic amplifier of at least one step of circuit, It has input capacitance, feedback capacity, and an operational amplifier, an inputted analog signal is amplified on a profit which becomes settled with a value of input capacitance, and a value of feedback capacity, and a switching means contains a variable region which sets either [at least] a value of input capacitance, or a value of feedback capacity as variable.
[0058]In this case, an inputted analog signal is amplified on a profit which becomes settled with a value of input capacitance, and a value of feedback capacity. Therefore, a profit of the 2nd arithmetic amplifier can be easily changed by changing either [at least] a value of input capacitance of an operational amplifier, or a value of feedback capacity.
[0059](7) In composition of an analog-to-digital circuit which requires an analog-to-digital circuit concerning invention the 7th invention of the 7th for the 6th invention, a variable region contains a switch part changed to a state or the state where it connected too hastily where a part of input capacitance or feedback capacity was separated.
[0060]In this case, input capacitance or feedback capacity of an operational amplifier can be changed by changing to a state or the state where it connected too hastily where a part of input capacitance or feedback capacity was separated by switch part. Thereby, a profit of the 2nd arithmetic amplifier can be changed easily.
[0061](8) An analog-to-digital circuit concerning the 8th invention invention of the 8th, In composition of an analog-to-digital circuit concerning the 3rd invention, the 1st arithmetic amplifier of at least one step of circuit, It has input capacitance, feedback capacity, and an operational amplifier, an inputted analog signal is amplified on a profit which becomes settled with a value of input capacitance, and a value of feedback capacity, and a switching means contains a variable region which sets either [at least] a value of input capacitance, or a value of feedback capacity as variable.
[0062]In this case, an inputted analog signal is amplified on a profit which becomes settled with a value of input capacitance, and a value of feedback capacity. Therefore, a profit of the 1st arithmetic amplifier can be easily changed by changing either [at least] a value of input capacitance of an operational amplifier, or a value of feedback capacity.
[0063](9) In composition of an analog-to-digital circuit which requires an analog-to-digital circuit concerning invention the 9th invention of the 9th for the 8th invention, a variable region contains a switch part changed to a state or the state where it connected too hastily where a part of input capacitance or feedback capacity was separated.
[0064]In this case, input capacitance or feedback capacity of an operational amplifier can be changed from changing to a state or the state where it connected too hastily where a part of input capacitance or feedback capacity was separated by switch part. Thereby, a profit of the 1st arithmetic amplifier can be changed easily.
[0065](10) An analog-to-digital circuit concerning the 10th invention invention of the 10th, In composition of an analog-to-digital circuit concerning the 9th invention, a switch part is connected to the 2nd capacity in series or in parallel including the 1st and 2nd capacity by which feedback capacity was provided in parallel or in series between an input terminal of an operational amplifier, and an output terminal.
[0066]If a switch part is made into a connected state, the 1st and 2nd capacity will be

connected in parallel or in series between an input terminal of an operational amplifier, and an output terminal. Thereby, feedback capacity increases or decreases. If a switch part is made into a cut off state, only the 1st capacity will be connected between an input terminal of an operational amplifier, and an output terminal. Thereby, feedback capacity decreases or increases.

[0067](11) A switch part is connected to an output terminal of an operational amplifier in composition of an analog-to-digital circuit which requires an analog-to-digital circuit concerning invention the 11th invention of the 11th for the 10th invention.
[0068]When the 2nd capacity is connected to an output side rather than a switch part, even if a switch part is set as a cut off state, parasitic capacitance of the 2nd capacity is charged. By that cause, it will be necessary to take parasitic capacitance into consideration, and a profit will vary with dispersion in parasitic capacitance at the time of setting out of a profit. Here, by connecting a switch part to an output side rather than the 2nd capacity, when a switch part is set as a cut off state, the 2nd capacity is separated from an output terminal by switch part with parasitic capacitance. Therefore, it becomes unnecessary to take parasitic capacitance of the 2nd capacity into consideration at the time of setting out of a profit, and dispersion in a profit by dispersion in parasitic capacitance is lost.
[0069](12) In composition of an analog-to-digital circuit which requires an analog-to-digital circuit concerning invention the 12th invention of the 12th for the 9th invention, input capacitance is provided in an input terminal of an operational amplifier in parallel or in series.
[0070]If a switch part is made into a connected state, the 1st and 2nd capacity will be connected to an input terminal of an operational amplifier in parallel or in series. Thereby, input capacitance increases or decreases. Only the 1st capacity will be connected to an input terminal of an operational amplifier if a switch part is made into a cut off state. Thereby, input capacitance decreases or increases.
[0071](13) A switch part is connected to an input side of the 2nd capacity in composition of an analog-to-digital circuit which requires an analog-to-digital circuit concerning invention the 13th invention of the 13th for the 12th invention.
[0072]When the 2nd capacity is connected to an input side rather than a switch part, even if a switch part is set as a cut off state, parasitic capacitance of the 2nd capacity is charged. By that cause, it will be necessary to take parasitic capacitance into consideration, and a profit will vary with dispersion in parasitic capacitance at the time of setting out of a profit. Here, by connecting a switch part to an input side rather than the 2nd capacity, when a switch part is set as a cut off state, it is separated from a node in which the 2nd capacity receives an input signal by a switch part with parasitic capacitance. Therefore, it becomes unnecessary to take parasitic capacitance of the 2nd capacity into consideration at the time of setting out of a profit, and dispersion in a profit by dispersion in parasitic capacitance is lost.
[0073](14) An analog-to-digital circuit concerning the 14th invention invention of the 14th, In composition of an analog-to-digital circuit concerning the 4th invention, an analog-digital converter of at least one step of circuit, A switching means contains a variable region which sets as variable two or more reference voltage generated by circuit generating reference voltage including circuit generating reference voltage which generates two or more reference voltage, and two or more comparators compared with an analog signal into which two or more reference voltage generated by circuit generating reference voltage was inputted.
[0074]In this case, a voltage range of reference voltage can be changed by changing reference voltage generated by circuit generating reference voltage. Thereby, a full-scale range of an analog-digital converter can be changed easily.
[0075](15) An analog-to-digital circuit concerning the 15th invention invention of the 15th, In composition of an analog-to-digital circuit concerning the 5th invention, a digital-to-analog converter of at least one step of circuit except a circuit of a final stage, Circuit generating reference voltage which generates reference voltage, and two or more capacity connected to a common terminal, Two or more switches which give reference voltage which was connected between circuit generating reference voltage and two or more capacity, and was generated by circuit generating reference voltage according to a digital signal inputted to two or more

capacity, respectively are included, A switching means contains a variable region which sets reference voltage generated by circuit generating reference voltage as variable.
[0076]In this case, a voltage range of reference voltage can be changed by changing reference voltage generated by circuit generating reference voltage. Thereby, a full-scale range of a digital-to-analog converter can be changed easily.
[0077]
[Embodiment of the Invention](1) The 1st embodiment drawing 1 is a block diagram showing the composition of the pipeline type analog-to-digital circuit in a 1st embodiment of this invention. The analog-to-digital circuit of drawing 1 has 10-bit four-step pipeline constitution.
[0078]In drawing 1, the analog-to-digital circuit 1 comprises the circuits 3-6, two or more latch circuitry 7, and the output circuit 8 of the 2 or 1st step - the 4th step of sample hold circuit.
[0079]The 1st (first rank) step of circuit 3 is provided with the arithmetic amplifier 11a, the subtractor circuit 12, and the arithmetic amplifier 13 which have sub A/D converter 9a which has a switchable full-scale range, D/A converter 10, and a switchable profit. The subtractor circuit 12 and the arithmetic amplifier 13 constitute the subtraction amplifier 14. The 2nd step and the 3rd step of circuits 4 and 5 are provided with sub A/D converter 9, D/A converter 10, the arithmetic amplifier 11, the subtractor circuit 12, and the arithmetic amplifier 13. The subtractor circuit 12 and the arithmetic amplifier 13 constitute the subtraction amplifier 14. The 4th (final stage) step of circuit 6 is provided only with sub A/D converter 9.
[0080]That the pipeline type analog-to-digital circuit 1 of drawing 1 differs from the conventional analog-to-digital circuit 100 of drawing 20, It is the point that the arithmetic amplifier 11a which has sub A/D converter 9a and the switchable profit which have a switchable full-scale range is used for the 1st step of circuit 3.
[0081]Here, the full-scale range of sub A/D converter 9 in the 1st step of circuit 3, It changes to voltage range VIN_{p-p} equal to it when the voltage range of an analog input signal is VIN_{p-p}, and when the voltage ranges of an analog input signal are $VIN_{p-p}/2$, it changes to voltage range $VIN_{p-p}/2$. [equal to it] The profit of the arithmetic amplifier 11a in the 1st step of circuit 3 is changed 1 time, when the voltage range of an analog input signal is VIN_{p-p}, and when the voltage ranges of an analog input signal are $VIN_{p-p}/2$, it is changed twice.
[0082]The full-scale range of D/A converter 10 in the 1st step - the 3rd step of circuit 3-5 is fixed, and the full-scale range of sub A/D converter 9 in the 2nd step - the 4th step of circuit 4-6 is being fixed. The profit of the arithmetic amplifiers 11 and 13 in the arithmetic amplifier 13 in the 1st step of circuit 3, the 2nd step, and the 3rd step of circuit 3 and 4 is 2.
[0083]4 bit configurations and the 2-4th step of circuits 4-6 of the 1st step of circuit 3 are 2 bit configurations, respectively. Similarly in the 1-3rd step of circuits 3-5, the number of bits (bit configuration) of sub A/D converters 9 and 9a and D/A converter 10 is set up.
[0084]Operation of the analog-to-digital circuit 1 of drawing 1 in case the voltage range of an analog input signal is VIN_{p-p}, and the voltage range of each part are the same as that of the analog-to-digital circuit 100 of drawing 20.
[0085]Here, operation of the analog-to-digital circuit 1 of drawing 1 in case the voltage ranges of an analog input signal are $VIN_{p-p}/2$, and the output voltage range of each part are explained.
[0086]The sample hold circuit 2 samples the analog input signal Vin, and carries out fixed time maintenance. The analog input signal Vin outputted from the sample hold circuit 2 is transmitted to the 1st step of circuit 3.
[0087]In the 1st step of circuit 3, sub A/D converter 9a performs an analog to digital to the analog input signal Vin of voltage range $VIN_{p-p}/2$. The full-scale range of sub A/D converter 9a at this time is changed to $VIN_{p-p}/2$ as mentioned above.
[0088]Top 4-bit digital output (2^9, 2^8, 2^7, 2^6) which is an A/D conversion result of sub A/D converter 9a is transmitted to the output circuit 8 via the four latch circuitry 7 while it is transmitted to D/A converter 10. D/A converter 10 changes into an analog signal top 4-bit digital output which is an A/D conversion result of sub A/D converter 9a.

[0089]Since the full-scale range of D/A converter 10 is being fixed to VIN_{p-p}, the normal output voltage range of D/A converter 10 is expressed like a following formula.
[0090]
(The 1st step of resolution-1) x(full-scale range of D/A converter 10)/(the 1st step of resolution)
$= (2^4-1) \times (VIN_{p-p}) / 2^4 = 15VIN_{p-p}/16$ one side and the arithmetic amplifier 11a sample the analog input signal Vin, and amplify and hold it. As mentioned above, since a profit is changed twice when the voltage ranges of an analog input signal are $VIN_{p-p}/2$, the output voltage range of the arithmetic amplifier 11a is expressed like a following formula.
[0091]
(Voltage range of the analog input signal Vin) x (profit of the arithmetic amplifier 11a)
$= (VIN_{p-p}/2)$ The x2 $=VIN_{p-p}$ subtraction amplifier 14 subtracts and amplifies the analog input signal Vin and the D/A conversion result of D/A converter 10 which were outputted from the arithmetic amplifier 11a. The output of the subtraction amplifier 14 is transmitted to the 2nd step of circuit 4.
[0092]The output voltage range of the 1st step of subtraction amplifier 14 is expressed like a following formula.
(Output voltage range of the arithmetic amplifier 11a) x (- (normal output voltage range of D/A converter 10)) (profit of the subtraction amplifier 14)
$= (VIN_{p-p}) (- (15VIN_{p-p}/16))$ In the x2 $=VIN_{p-p}/82$ step circuit 4, sub A/D converter 9 performs an A/D conversion to the output of the subtraction amplifier 14 of the 1st step of circuit 3. The A/D conversion result of sub A/D converter 9 is transmitted to the output circuit 8 via the three latch circuitry 7 while it is transmitted to D/A converter 10. Thereby, a 2-bit digital output (2^5, 2^4) is obtained at least for Nakagami from the 2nd step of circuit 4.
[0093]On the other hand, the arithmetic amplifier 11 amplifies the output of the subtraction amplifier 14 of the 1st step of circuit 3. The subtraction amplifier 14 subtracts and amplifies the output of the arithmetic amplifier 11, and the D/A conversion result of D/A converter 10. The output of the subtraction amplifier 14 is transmitted to the 3rd step of circuit 5.
[0094]In the 3rd step of circuit 5, the same operation as the 2nd step of circuit 4 is performed to the output of the subtraction amplifier 14 of the 2nd step of circuit 4. Thereby, a 2-bit digital output (2^3, 2^2) is obtained at least for Nakashita from the 3rd step of circuit 5.
[0095]In the 4th step of circuit 6, sub A/D converter 9 performs an A/D conversion to the output of the subtraction amplifier 14 of the 3rd step of circuit 5, and the digital output (2^1, 2^0) of 2 bits of low ranks is obtained.
[0096]The digital output of the 1st step - the 4th step of circuits 3-6 arrives at the output circuit 8 simultaneously through each latch circuitry 7. That is, each latch circuitry 7 is formed in order to take the synchronization of the digital output of each circuits 3-6.
[0097]The output circuit 8 carries out the after [a digital compensation process] parallel output of the 10-bit digital output Dout of the analog input signal Vin, when required.
[0098]As mentioned above, when the voltage ranges of an analog input signal are $VIN_{p-p}/2$. By changing the full-scale range of the profit of the arithmetic amplifier 11a of the 1st step of circuit 3, and sub A/D converter 9a of the 1st step of circuit 3, The voltage range of the output signal given in the 2nd step of circuit 5 is set to $VIN_{p-p}/8$ from the subtraction amplifier 14 of the 1st step of circuit 3 like the case where the voltage range of an analog input signal is VIN_{p-p}. Thereby, although the voltage range of the analog input signal Vin became half, the digital output same before the voltage range of an analog input signal becomes half is obtained.
[0099]Therefore, the analog-to-digital circuit corresponding to change of the voltage range of an analog input signal can be provided, without changing a circuit design.
[0100]According to this embodiment, the analog-to-digital circuit of a differential double end input method can be changed into the analog-to-digital circuit of a single-ended input method,

without changing circuitry.
[0101]Drawing 2 (a) and (b) is a figure showing setting out in the case of changing the analog-to-digital circuit 1 of drawing 1 to a differential double end input method and a single-ended input method, respectively.
[0102]As shown in drawing 2 (a), at the time of a differential double end input, the profit of the arithmetic amplifier 11a is changed 1 time, and the full-scale range of sub A/D converter 9a is changed to $2VIN_{p-p}$. In this example, the right side analog input voltage Vin of the analog input signal Vin of a differential double end input (+) changes in 1.0V to 2.0V, and the negative side analog input voltage Vin (-) changes from 2.0V in 1.0V. The voltage range of the analog input signal Vin becomes like a following formula.
[0103]The maximum of $2VIN_{p-p}$= [Vin(+)-Vin (-)] - minimum =2.0 [V] of [Vin(+)-Vin (-)]
In this case, the right side reference voltage Vref of sub A/D converter 9a (+) changes in 1.0V to 2.0V, and the negative side reference voltage Vref (-) changes from 2.0V in 1.0V.
[0104]As shown in drawing 2 (b), at the time of a single-ended input, the profit of the arithmetic amplifier 11a is changed twice, and the full-scale range of sub A/D converter 9a is changed to VIN_{p-p}. The right side analog input voltage Vin of the analog input signal Vin of the single-ended input in this example (+) changes in 1.0V to 2.0V, and that of the negative side analog input voltage Vin (-) is constant 1.5V. The voltage range of the analog input signal Vin becomes like a following formula.
[0105]The maximum of VIN_{p-p}= [Vin(+)-Vin (-)] - minimum =1.0 [V] of [Vin(+)-Vin (-)]
In this case, the right side reference voltage Vref of sub A/D converter 9a (+) changes in 1.0V to 2.0V, and its negative side reference voltage Vref (-) is constant 1.5V.
[0106]Thus, in the analog-to-digital circuit 1 of drawing 1, even if the voltage range of an analog input signal is set to one half by changing a differential double end input method into a single-ended input method, redesign of circuitry becomes unnecessary.
[0107]Redesign of circuitry becomes unnecessary, when changing the voltage range of the analog input signal of a single-ended input into one half, and also when changing the voltage range of the analog input signal of a differential double end input into one half.
[0108]Thus, in the same LSI (large scale integration circuit), the voltage range of the output of an analog input signal and an arithmetic amplifier, the output of a D/A conversion circuit, and the output of a subtraction amplifier can be changed programmably. As a result, while being able to attain shortening of a development cycle, it is also possible to perform low power consumption.
[0109](2) The 2nd embodiment drawing 3 is a block diagram showing the composition of the pipeline type analog-to-digital circuit in a 2nd embodiment of this invention. The analog-to-digital circuit 1 of drawing 3 also has 10-bit four-step pipeline constitution.
[0110]In drawing 3, the analog-to-digital circuit 1 comprises the circuits 3-6, two or more latch circuitry 7, and the output circuit 8 of the 2 or 1st step - the 4th step of sample hold circuit.
[0111]4 bit configurations and the 2-4th step of circuits 4-6 of the 1st step of circuit 3 are 2 bit configurations, respectively. Similarly in the 1-3rd step of circuits 3-5, the number of bits (bit configuration) of sub A/D converters 9 and 9b and D/A converters 10 and 10b is set up.
[0112]The 1st (first rank) step of circuit 3 is provided with the arithmetic amplifier 13a which has sub A/D converter 9, D/A converter 10, the arithmetic amplifier 11, the subtractor circuit 12, and a switchable profit. The subtractor circuit 12 and the arithmetic amplifier 13a constitute the subtraction amplifier 14a.
[0113]The 2nd step and the 3rd step of circuits 4 and 5 are provided with sub A/D converter 9b which has a switchable full-scale range, D/A converter 10b which has a switchable full-scale range, the arithmetic amplifier 11, the subtractor circuit 12, and the arithmetic amplifier 13. The subtractor circuit 12 and the arithmetic amplifier 13 constitute the subtraction amplifier 14. The 4th (final stage) step of circuit 6 is provided only with sub A/D converter 9b which has a switchable full-scale range.
[0114]Here, the 2nd step - the 4th step of sub A/D converter 9b shall have the 2nd step - the 4th step of A/D converter 9 of drawing 20 twice the accuracy of sub. Redesign of the analog-

to-digital circuit 1 at the time of using for the 2nd step - the 4th step hereafter sub A/D converter 9b which has twice as many accuracy as this is explained.

[0115]It is switchable 1 time and twice in the profit of the subtraction amplifier 14a in the 1st step of circuit 3. It is switchable to $VIN_{p-p}/8$, and $VIN_{p-p}/16$ in the full-scale range of sub A/D converter 9b in the 2nd step - the 4th step of circuit 4-6. It is switchable to $VIN_{p-p}/4$, and $VIN_{p-p}/8$ in the full-scale range of D/A converter 10b in the 2nd step and the 3rd step of circuit 4 and 5.

[0116]Here, the profit of the subtraction amplifier 14a in the 1st step of circuit 3 is changed 1 time. The full-scale range of sub A/D converter 9b in the 2nd step - the 4th step of circuit 4-6 is changed to $VIN_{p-p}/16$, and the full-scale range of D/A converter 10b in the 2nd step and the 3rd step of circuit 4 and 5 is changed to $VIN_{p-p}/8$. The full-scale range of sub A/D converter 9 in the 1st step of circuit 3 is VIN_{p-p}. The profit of the arithmetic amplifiers 11 and 13 in the 2nd step and the 3rd step of circuit 3 and 4 is 2.

[0117]Here, operation of the analog-to-digital circuit 1 of drawing 1 in case the voltage range of an analog input signal is VIN_{p-p}, and the output voltage range of each part are explained.

[0118]The sample hold circuit 2 samples the analog input signal Vin, and carries out fixed time maintenance. The analog input signal Vin outputted from the sample hold circuit 2 is transmitted to the 1st step of circuit 3.

[0119]In the 1st step of circuit 3, sub A/D converter 9 performs an analog to digital to the analog input signal Vin of voltage range VIN_{p-p}. The full-scale range of sub A/D converter 9 at this time is VIN_{p-p}.

[0120]Top 4-bit digital output (2^9, 2^8, 2^7, 2^6) which is an A/D conversion result of sub A/D converter 9 is transmitted to the output circuit 8 via the four latch circuitry 7 while it is transmitted to D/A converter 10. D/A converter 10 changes into an analog signal top 4-bit digital output which is an A/D conversion result of sub A/D converter 9.

[0121]Since the full-scale range of D/A converter 10 is being fixed, the normal output voltage range of D/A converter 10 is expressed like a following formula.

[0122]

(The 1st step of resolution-1) x(full-scale range of D/A converter 10)/(the 1st step of resolution)

$= (2^4-1) \times (VIN_{p-p}) / 2^4 = 15VIN_{p-p}/16$ one side and the arithmetic amplifier 11 sample the analog input signal Vin, and amplify and hold it. Since the profit of the arithmetic amplifier 11 is 1 time, the output voltage range of the arithmetic amplifier 11 is expressed like a following formula.

[0123]

(Voltage range of the analog input signal Vin) x (profit of the arithmetic amplifier 11)

$= \text{The } VIN_{p-p} \times 1 = VIN_{p-p}$ subtraction amplifier 14a subtracts and amplifies the analog input signal Vin and the D/A conversion result of D/A converter 10 which were outputted from the arithmetic amplifier 11. The output of the subtraction amplifier 14a is transmitted to the 2nd step of circuit 4.

[0124]Since the profit of the 1st step of subtraction amplifier 14a is changed to 1, the output voltage range of the 1st step of subtraction amplifier 14a is expressed like a following formula.

[0125]

(Output voltage range of the arithmetic amplifier 11) x (- (normal output voltage range of D/A converter 10)) (profit of the subtraction amplifier 14a)

$= (VIN_{p-p}) (- (15VIN_{p-p}/16))$ In the $\times 1 = VIN_{p-p}/162$ step circuit 4, sub A/D converter 9b performs an A/D conversion to the output of the subtraction amplifier 14a of the 1st step of circuit 3. The A/D conversion result of sub A/D converter 9b is transmitted to the output circuit 8 via the three latch circuitry 7 while it is transmitted to D/A converter 10b.

[0126]In this case, since sub A/D converter 9b has A/D converter 9 of drawing 20 twice the accuracy of sub, A 2-bit digital output (2^5, 2^4) is obtained at least for Nakagami from the 2nd step of circuit 4 by full-scale range $VIN_{p-p}/16$ of the half of sub A/D converter 9 of drawing 20.
[0127]At least Nakagami whose D/A converter 10b is an A/D conversion result of sub A/D converter 9b changes a 2-bit digital output into an analog signal.
[0128]Since the full-scale range of D/A converter 10b is changed to $VIN_{p-p}/8$ of the half of D/A converter 10 of drawing 20, the normal output voltage range of D/A converter 10b is expressed like a following formula.
[0129]
(The 2nd step of resolution-1) x (full-scale range of D/A converter 10b)
/(the 2nd step of resolution)
= (2^2-1) x ($VIN_{p-p}/8$) / 2^2=$3VIN_{p-p}/32$ one side and the arithmetic amplifier 11 amplify the output of the subtraction amplifier 14a of the 1st step of circuit 3. As mentioned above, since the profit of the subtraction amplifier 14a of the 1st step of circuit 3 is changed to 1, the output voltage range of the arithmetic amplifier 11a is expressed like a following formula.
[0130]
(Output voltage range of the 1st step of subtraction amplifier 14a) x (profit of the arithmetic amplifier 11)
= ($VIN_{p-p}/16$) The x2 =$VIN_{p-p}/8$ subtraction amplifier 14 subtracts and amplifies the output of the arithmetic amplifier 11, and the D/A conversion result of D/A converter 10b. The output of the subtraction amplifier 14 is transmitted to the 3rd step of circuit 5.
[0131]The output voltage range of the 2nd step of subtraction amplifier 14 is expressed like a following formula.
(Output voltage range of the arithmetic amplifier 11) x (- (normal output voltage range of D/A converter 10b)) (profit of the subtraction amplifier 14)
= ($VIN_{p-p}/8$) (- ($3VIN_{p-p}/32$)) In the x2 =$VIN_{p-p}/163$ step circuit 5, the same operation as the 2nd step of circuit 4 is performed to the output of the subtraction amplifier 14 of the 2nd step of circuit 4. In this case, since sub A/D converter 9b has A/D converter 9 of drawing 20 twice the accuracy of sub, A 2-bit digital output (2^3, 2^2) is obtained at least for Nakashita from the 3rd step of circuit 5 by full-scale range $VIN_{p-p}/16$ of the half of sub A/D converter 9 of drawing 20. The output voltage range of each part is the same as that of the 2nd step of circuit 4.
[0132]In the 4th step of circuit 6, sub A/D converter 9b performs an A/D conversion to the output of the subtraction amplifier 14 of the 3rd step of circuit 5. In this case, since sub A/D converter 9b has A/D converter 9 of drawing 20 twice the accuracy of sub, The digital output (2^1, 2^0) of 2 bits of low ranks is obtained from the 4th step of circuit 6 by full-scale range $VIN_{p-p}/16$ of the half of sub A/D converter 9 of drawing 20.
[0133]The digital output of the 1st step - the 4th step of circuits 3-6 arrives at the output circuit 8 simultaneously through each latch circuitry 7. That is, each latch circuitry 7 is formed in order to take the synchronization of the digital output of each circuits 3-6.
[0134]The output circuit 8 carries out the after [a digital compensation process] parallel output of the 10-bit digital output Dout of the analog input signal Vin, when required.
[0135]As mentioned above, in the analog-to-digital circuit 1 of drawing 3. Although the voltage range of each part of the circuits 4-6 after the 2nd step became half [of the analog-to-digital circuit 100 of drawing 20] by using sub A/D converter 9b which has twice as many accuracy as this, the digital output same before a voltage range becomes half is obtained.
[0136]In this case, the alternating current component of current which flows through the circuits 3-6 of each stage decreases by optimizing a voltage range to sub A/D converter 9b which has twice as many accuracy as this, and setting it as a half. Thereby, the consumed electric current can provide the analog-to-digital circuit by which reduction was carried out by optimizing a voltage range, without changing a circuit design.

[0137](3) Circuitry drawing 4 of each part is a circuit diagram showing the 1st example of the composition of the arithmetic amplifier 11a in the analog-to-digital circuit 1 of drawing 1.
[0138]The arithmetic amplifier 11a of drawing 4 includes the operational amplifier 110, the capacity value switching circuit 111,112, the capacitor 113,114, and the switches 115-122. The switches 115-122 are constituted by the MOS (metal oxide semiconductor) transistor, for example.
[0139]The capacity value switching circuit 111 is connected as feed back capacity between the inversed input terminal of the operational amplifier 110, and an inverted output terminal, and the capacity value switching circuit 112 is connected as feed back capacity between the non-inversed input terminal and the noninverting output terminal. The capacitor 113 is connected to the inversed input terminal of the operational amplifier 110 as input capacitance, and the capacitor 114 is connected to the non-inversed input terminal as input capacitance.
[0140]The right side analog input voltage Vin (+) and middle reference voltage VRT1 are given to the capacitor 113 via the switch 115,116, respectively. The negative side analog input voltage Vin (-) and middle reference voltage VRT1 are given to the capacitor 114 via the switch 117,118, respectively. The inversed input terminal, the inverted output terminal, non-inversed input terminal, and noninverting output terminal of the operational amplifier 110 are grounded via the switch 119,120,121,122, respectively.
[0141]If capacity value of the capacitor 113,114 is set to CA, respectively and capacity value of the capacity value switching circuit 111,112 is set to CB here, respectively, The right side analog output voltage Vo of the inverted output terminal of the operational amplifier 110 (+) and the negative side analog output voltage Vo of a noninverting output terminal (-) become like a following formula.
[0142]
Vo(+) = (Vin(+)-VRT1) and (CA/CB)
Vo(-) = (Vin(-)-VRT1) and (CA/CB)
deltaVo=Vo(+)-Vo (-)
= (Vin(+)-Vin (-)) -(CA/CB)
Therefore, the profit of the arithmetic amplifier 11a can be changed by changing the capacity value CB of the capacity value switching circuit 111,112.
[0143]Drawing 5 is a circuit diagram showing the 2nd example of the composition of the arithmetic amplifier 11a in the analog-to-digital circuit 1 of drawing 1.
[0144]The arithmetic amplifier 11a of drawing 5 includes the operational amplifier 110, the capacitor 123,124, the capacity value switching circuit 125,126, and the switches 115-122.
[0145]The capacitor 123 is connected as feed back capacity between the inversed input terminal of the operational amplifier 110, and an inverted output terminal, and the capacitor 124 is connected as feed back capacity between the non-inversed input terminal and the noninverting output terminal. The capacity value switching circuit 125 is connected to the inversed input terminal of the operational amplifier 110 as input capacitance, and the capacity value switching circuit 126 is connected to the non-inversed input terminal as input capacitance.
[0146]The right side analog input voltage Vin (+) and middle reference voltage VRT1 are given to the capacity value switching circuit 125 via the switch 115,116, respectively. The negative side analog input voltage Vin (-) and middle reference voltage VRT1 are given to the capacity value switching circuit 126 via the switch 117,118, respectively. The inversed input terminal, the inverted output terminal, non-inversed input terminal, and noninverting output terminal of the operational amplifier 110 are grounded via the switch 119,120,121,122, respectively.
[0147]If capacity value of the capacity value switching circuit 125,126 is set to CC, respectively and capacity value of the capacitor 123,124 is set to CD here, respectively, The right side analog output voltage Vo of the inverted output terminal of the operational amplifier 110 (+) and the negative side analog output voltage Vo of a noninverting output terminal (-) become like a following formula.
[0148]
Vo(+) = (Vin(+)-VRT1) and (CC/CD)
Vo(-) = (Vin(-)-VRT1) and (CC/CD)

deltaVo=Vo(+)-Vo (-)
= (Vin(+)-Vin (-)) -(CC/CD)
Therefore, the profit of the arithmetic amplifier 11a can be changed by changing capacity value CC of the capacity value switching circuit 125,126.
[0149]Drawing 6 - drawing 11 are the circuit diagrams showing the 1st - the 6th example of the concrete circuitry of the arithmetic amplifier 11a.
[0150]In drawing 6 - drawing 11, each of the capacitors Ca, Cb, and Cc shall have the equal capacity value C. Let m be arbitrary positive integers.
[0151]In the example of drawing 6, the parallel circuit and the switch Sa of m capacitor Ca are connected in series between the inversed input terminal of the operational amplifier 110, and an inverted output terminal, and the parallel circuit of m capacitor Ca is connected. Here, m is arbitrary positive integers. Similarly, the parallel circuit and the switch Sa of m capacitor Ca are connected in series between the non-inversed input terminal of the operational amplifier 110, and a noninverting output terminal, and the parallel circuit of m capacitor Ca is connected. The 2m piece capacitor Cb is connected to the inversed input terminal of the operational amplifier 110, and the 2m piece capacitor Cb is connected to the non-inversed input terminal.
[0152]The right side analog input voltage Vin (+) is given to the 2m piece capacitor Cb by the side of an inversed input terminal via the switch S1, respectively. The negative side analog input voltage Vin (-) is given to the capacitor Cb by the side of a non-inversed input terminal via the switch S1, respectively. The high potential side reference voltage VRT is given to the m capacitors Cb by the side of an inversed input terminal, and the m capacitors Cb by the side of a non-inversed input terminal via the switch S2, respectively, The low voltage side reference voltage VRB is given to the m capacitors Cb by the side of a non-inversed input terminal, and the m capacitors Cb by the side of a non-inversed input terminal via the switch S2, respectively.

[0153]In this example, the values of input capacitance are 2mC. If the switch Sa is carried out to one, the value of feed back capacity will serve as 2mC, and if the switch Sa is turned OFF, the value of feed back capacity will serve as mC. Therefore, at the time of a differential double end input, by changing the switch Sa to one, a profit will be 1 time and a profit will be twice by changing the switch Sa to OFF at the time of a single-ended input.
[0154]In the example of drawing 7, the parallel circuit of 2m piece capacitor Ca and the parallel circuit of 2m piece capacitor Cc are connected in series between the inversed input terminal of the operational amplifier 110, and an inverted output terminal, and the switch Sa is connected in parallel with capacitor Cc. Similarly, the parallel circuit of 2m piece capacitor Ca and the parallel circuit of 2m piece capacitor Cc are connected in series between the non-inversed input terminal of the operational amplifier 110, and a noninverting output terminal, and the switch Sa is connected in parallel with capacitor Cc. The composition of other portions of the arithmetic amplifier 11a of drawing 7 is the same as that of the arithmetic amplifier 11a of drawing 6.
[0155]In this example, the values of input capacitance are 2mC. If the switch Sa is carried out to one, the value of feed back capacity will serve as 2mC, and if the switch Sa is turned OFF, the value of feed back capacity will serve as mC. Therefore, at the time of a differential double end input, by changing the switch Sa to one, a profit will be 1 time and a profit will be twice by changing the switch Sa to OFF at the time of a single-ended input.
[0156]In the example of drawing 8, the parallel circuit of 2m piece capacitor Ca and the parallel circuit of 2m piece capacitor Cc are connected in series between the inversed input terminal of the operational amplifier 110, and an inverted output terminal, and the switch Sa is connected in parallel with capacitor Ca. Similarly, the parallel circuit of 2m piece capacitor Ca and the parallel circuit of 2m piece capacitor Cc are connected in series between the non-inversed input terminal of the operational amplifier 110, and a noninverting output terminal, and the switch Sa is connected in parallel with capacitor Ca. The composition of other portions of the arithmetic amplifier 11a of drawing 8 is the same as that of the arithmetic amplifier 11a of drawing 6.
[0157]In this example, the values of input capacitance are 2mC. If the switch Sa is carried out to one, the value of feed back capacity will serve as 2mC, and if the switch Sa is turned OFF, the value of feed back capacity will serve as mC. Therefore, at the time of a differential double end

input, by changing the switch Sa to one, a profit will be 1 time and a profit will be twice by changing the switch Sa to OFF at the time of a single-ended input.
[0158]In the example of drawing 9, the parallel circuit of m capacitor Ca is connected between the inversed input terminal of the operational amplifier 110, and the inverted output terminal. Similarly, the parallel circuit of m capacitor Ca is connected between the non-inversed input terminal of the operational amplifier 110, and the noninverting output terminal. The 2m piece capacitor Cb is connected to the inversed input terminal of the operational amplifier 110, and the 2m piece capacitor Cb is connected to the non-inversed input terminal.
[0159]The right side analog input voltage Vin (+) is given to the 2m piece capacitor Cb by the side of an inversed input terminal via the switch S1 and S1a, respectively. The negative side analog input voltage Vin (-) is given to the capacitor Cb by the side of a non-inversed input terminal via the switch S1 and S1a, respectively. The high potential side reference voltage VRT is given to the m capacitors Cb by the side of an inversed input terminal, and the m capacitors Cb by the side of a non-inversed input terminal via the switch S2 and S2a, respectively, The low voltage side reference voltage VRB is given to the m capacitors Cb by the side of a non-inversed input terminal, and the m capacitors Cb by the side of a non-inversed input terminal via the switch S2 and S2a, respectively.
[0160]In this example, the value of feed back capacity is mC. If the switch S1a and S2a are made one, the value of input capacitance will serve as 2mC, and if the switch S1a and S2a are turned OFF, the value of input capacitance will serve as mC. Therefore, at the time of a differential double end input, by always turning OFF the switch S1a and S2a, a profit will be 1 time and a profit will be twice by carrying out switching operation of the switch S1a and the S2a like the switch S1 and S2 at the time of a single-ended input.
[0161]In the example of drawing 10, the parallel circuit of m capacitor Ca is connected between the inversed input terminal of the operational amplifier 110, and the inverted output terminal. Similarly, the parallel circuit of m capacitor Ca is connected between the non-inversed input terminal of the operational amplifier 110, and the noninverting output terminal. The parallel circuit of 2m piece capacitor Cc is connected to the inversed input terminal of the operational amplifier 110, the 2m piece capacitor Cb is connected to the parallel circuit of capacitor Cc, and the switch Sa is connected in parallel with capacitor Cc. The parallel circuit of 2m piece capacitor Cc is connected to a non-inversed input terminal, the 2m piece capacitor Cb is connected to the parallel circuit of capacitor Cc, and the switch Sa is connected in parallel with capacitor Cc. The composition of other portions of the arithmetic amplifier 11a of drawing 10 is the same as that of the arithmetic amplifier 11a of drawing 6.
[0162]In this example, the value of feed back capacity is mC. If the switch Sa is carried out to one, the value of input capacitance will serve as 2mC, and if the switch Sa is turned OFF, the value of input capacitance will serve as mC. Therefore, at the time of a differential double end input, by turning OFF the switch Sa, a profit will be 1 time and a profit will be twice by carrying out the switch Sa to one at the time of a single-ended input.
[0163]In the example of drawing 11, the parallel circuit of m capacitor Ca is connected between the inversed input terminal of the operational amplifier 110, and the inverted output terminal. Similarly, the parallel circuit of m capacitor Ca is connected between the non-inversed input terminal of the operational amplifier 110, and the noninverting output terminal. The parallel circuit of 2m piece capacitor Cc is connected to the inversed input terminal of the operational amplifier 110, the 2m piece capacitor Cb is connected to the parallel circuit of capacitor Cc, and the switch Sa is connected to the capacitor Cb in parallel. The parallel circuit of 2m piece capacitor Cc is connected to a non-inversed input terminal, the 2m piece capacitor Cb is connected to the parallel circuit of capacitor Cc, and the switch Sa is connected to the capacitor Cb in parallel. The composition of other portions of the arithmetic amplifier 11a of drawing 11 is the same as the composition of the arithmetic amplifier 11a of drawing 6.
[0164]In this example, the value of feed back capacity is mC. If the switch Sa is carried out to one, the value of input capacitance will serve as 2mC, and if the switch Sa is turned OFF, the value of input capacitance will serve as mC. Therefore, at the time of a differential double end input, by turning OFF the switch Sa, a profit will be 1 time and a profit will be twice by carrying

out the switch Sa to one at the time of a single-ended input.
[0165]In the arithmetic amplifier 11a of drawing 6 - drawing 11, the switch Sa is constituted by the MOS transistor as mentioned above. The diffusion capacitance of a MOS transistor is added to the node to which the switch Sa is connected by that cause, and gate capacitance is added at the time of one of the switch Sa. If capacity is added to the inversed input terminal or non-inversed input terminal of the operational amplifier 110, the working speed of the arithmetic amplifier 11a will fall.
[0166]The switch Sa is connected to the inverted output terminal and noninverting output terminal of the operational amplifier 110 in the example of drawing 6 and drawing 7. Thereby, the working speed of the arithmetic amplifier 11a does not fall. Therefore, the example of drawing 6 and drawing 7 is preferred.
[0167]Since on resistance exists at the time of one of the switch Sa when the switch Sa is connected in parallel with a capacitor, the capacity of a capacitor is thoroughly unseparable.
[0168]In the example of drawing 6, the switch Sa is connected to capacitor Ca in series, and the switch Sa is connected to the inverted output terminal and noninverting output terminal of the operational amplifier 110. Thereby, the capacity of capacitor Ca is thoroughly separable at the time of one of the switch Sa. Therefore, the example of drawing 6 is the most preferred.
[0169]In the example of drawing 9, the switch S1a and S2a are connected to the input side rather than the capacitor Cb. On the contrary, when the capacitor Cb is connected to the input side rather than the switch S1a and S2a, even if the switch S1a and S2a are set as an OFF state, the parasitic capacitance of the capacitor Cb is charged. By that cause, it will be necessary to take parasitic capacitance into consideration, and a profit will vary with dispersion in parasitic capacitance at the time of setting out of a profit. Like the example of drawing 9, by connecting the switch S1a and S2a to an input side rather than the capacitor Cb, when the switch S1a and S2a are set as an OFF state, the capacitor Cb is separated by the switch S1a and S2a with parasitic capacitance. Therefore, in the example of drawing 9, it becomes unnecessary to take the parasitic capacitance of the capacitor Cb into consideration at the time of setting out of a profit, and dispersion in the profit by dispersion in parasitic capacitance is lost.
[0170]The circuit diagram showing the 1st example of the composition of sub A/D converter [in / in drawing 12 / the analog-to-digital circuit 1 of drawing 1] 9a and drawing 13 are the circuit diagrams showing the composition of the comparator used for sub A/D converter 9a of drawing 12.
[0171]Sub A/D converter 9a is provided with the circuit generating reference voltage 92, 93a, and 93b and two or more comparators 90 which generate reference voltage in drawing 12.
[0172]The circuit generating reference voltage 92 consists of two or more resistance R connected in series. The circuit generating reference voltage 93a consists of two or more resistance R connected in series. The circuit generating reference voltage 93b consists of two or more resistance R1 connected in series. Two or more resistance R has equal resistance, and two or more resistance R1 has equal resistance.
[0173]The circuit generating reference voltage 92 is connected between the node N91 which receives the high potential side reference voltage VRT, and the node N92 which receives the low voltage side reference voltage VRB. The circuit generating reference voltage 93a is connected via the switch S24 and S25 between the node N93 which receives the high potential side reference voltage VRT, and the node N94 which receives the low voltage side reference voltage VRB. The circuit generating reference voltage 93b is connected between the node N93 which receives the high potential side reference voltage VRT, and the node N94 which receives the low voltage side reference voltage VRB. The switch S26 is connected between the intermediate node N95 of the circuit generating reference voltage 93a, and the intermediate node N96 of the circuit generating reference voltage 93b.
[0174]Reference voltage which is different at the node during the resistance R of the circuit generating reference voltage 92, respectively is generated. Similarly, reference voltage which is different at the node during the resistance R of the circuit generating reference voltage 93a, respectively is generated. Here, different reference voltage obtained by the circuit generating

reference voltage 92 is called the right side reference voltage Vref (+). Different reference voltage obtained by the circuit generating reference voltage 93a is called the negative side reference voltage Vref (−).
[0175]Middle reference voltage VRT1 (=(VRT−VRB)/2) which is the middle voltage of the high potential side reference voltage VRT and the low voltage side reference voltage VRB is generated by the intermediate node N96 of the circuit generating reference voltage 93b.
[0176]As shown in drawing 13, each comparator 90 includes the operational amplifier 91, the capacitor C1, C2, and the switches S13−S18. The switch S13 is connected between the inversed input terminal of the operational amplifier 91, and an inverted output terminal, and the switch S14 is connected between the non−inversed input terminal and the noninverting output terminal. The capacitor C1 is connected to the inversed input terminal of the operational amplifier 91, and the capacitor C2 is connected to the non−inversed input terminal. The switch S15 and S16 are connected to the capacitor C1, and the switch S17 and S18 are connected to the capacitor C2. In drawing 12, the switch S13 of each comparator 90 and the graphic display of S14 are omitted.
[0177]The right side analog input voltage Vin (+) and the right side reference voltage Vref (+) are given to the capacitor C1 via the switch S15 and S16, respectively. The negative side analog input voltage Vin (−) and the negative side reference voltage Vref (−) are given to the capacitor C2 via the switch S17 and S18, respectively.
[0178]In the initial state, and the switch S16 and S18 turn off. [the switch S13 S14, S15, and S17] Next, the one [the switch S15 and S17 are turned off and / the switch S16 and S18] after turning off the switch S13 and S14. Since the inversed input terminal and non−inversed input terminal of the operational amplifier 91 are floating when the switch S13 and S14 are turned off, The voltage of an inversed input terminal changes (Vin(+)−Vref (+)), and the voltage of a non−inversed input terminal changes (Vin(−)−Vref (−)). As a result, differential analog input voltage (Vin(+)−Vin (−)) and differential reference voltage (Vref(+)−Vref (−)) are measured, and right side analog−output−voltage Vout (+) and negative side analog−output−voltage Vout (−) change according to a comparison result.
[0179]The digital code Dcode can be obtained by encoding the comparison result of two or more comparators 90 of drawing 12 with the encoder 950.
[0180]In sub A/D converter 9a of drawing 12, at the time of a differential double end input, and the switch S26 is turned off. [the switch S24 and S25] Thereby, the negative side reference voltage Vref (−) which changes with circuit generating reference voltage 93a via the switch S18, respectively to the capacitor C2 of each comparator 90 is given. At the time of a single−ended input, the switch S24 and S25 are turned off and the switch S26 is carried out to one. Thereby, middle reference voltage VRT1 is given to the capacitor C2 of each comparator 90 by the circuit generating reference voltage 93b via the switch S18.
[0181]Thus, a full−scale range is changed in sub A/D converter 9a.
[0182]The switch S26 may be connected between the intermediate node N95 of the circuit generating reference voltage 93a, and the intermediate node of the circuit generating reference voltage 92, without forming the circuit generating reference voltage 93b.
[0183]The circuit diagram showing the 2nd example of the composition of sub A/D converter [in / in drawing 14 / the analog−to−digital circuit 1 of drawing 1] 9a and drawing 15 are the circuit diagrams showing the composition of the comparator used for sub A/D converter 9a of drawing 14.
[0184]In drawing 14, the switch S26 of drawing 12 is not connected between the intermediate node N95 of the circuit generating reference voltage 93a, and the intermediate node N96 of the circuit generating reference voltage 93b.
[0185]As shown in drawing 15, each comparator 90 includes the operational amplifier 91, the capacitor C1, C2, and the switches S13−S18, and contains the switch S21 and S22 further. One end of the switch S21 is connected to the capacitor C1, and the other end of the switch S21 is opened wide. One end of the switch S22 is connected to the capacitor C2, and the other end is connected to the intermediate node N96 of the reference voltage generating time 93b of drawing 14. The composition of other portions of the comparator 90 of drawing 15 is the same as the composition of the comparator 90 of drawing 13.

[0186]Middle reference voltage VRT1 is given to the capacitor C2 by the reference voltage generating time 93b via the switch S22.
[0187]Operation of the comparator 90 of drawing 15 at the time of a differential double end input is the same as operation of the comparator 90 of drawing 13. At this time, the switch S21 and S22 are always turned off. At the time of a single-ended input, the switch S22 is operated instead of the switch S18. At this time, the switch S21 is always turned off.
[0188]The one [the switch S24 and S25] at the time of a differential double end input in sub A/D converter 9a of drawing 14. At this time, the switch S21 and S22 are always turned OFF. Thereby, the negative side reference voltage Vref (-) which changes with circuit generating reference voltage 93a via the switch S18, respectively to the capacitor C2 of each comparator 90 is given. At the time of a single-ended input, the switch S24 and S25 are turned off and the switch S22 is operated instead of the switch S18. At this time, the switch S21 is always turned off. Thereby, middle reference voltage VRT1 is given to the capacitor C2 of each comparator 90 by the circuit generating reference voltage 93b via the switch S22.
[0189]Thus, a full-scale range is changed in sub A/D converter 9a.
[0190]Although it is not necessary to form the switch S21 in each comparator 90, in order to secure the symmetry of the circuitry of the comparator 90, it is preferred to form the switch S21.
[0191]Drawing 16 is a circuit diagram of sub A/D converter 9b in the 2nd step of circuit 4 in the analog-to-digital circuit 1 of drawing 3. Sub A/D converter 9b of drawing 16 is a full-parallel comparison (flash plate) method sub A/D converter.
[0192]Sub A/D converter 9b comprises the circuit generating reference voltage 94 and 95 and two or more comparators 90 which generate reference voltage. Each of the circuit generating reference voltage 94 and 95 consists of the resistance R2 or 2n resistance R of a piece and, and the resistance R3. The resistance R2 and R3 have resistance n times the resistance of R, respectively. The resistance R2 or 2n resistance R of a piece and, and the resistance R3 are connected between the node N97 which receives high potential side reference voltage VRT2, and the node N98 which receives low voltage side reference voltage VRB2. The switch S28 is connected to the both ends of the resistance R2, and the switch S29 is connected to the both ends of the resistance R3.
[0193]Reference voltage which is different at the node during the resistance R of the circuit generating reference voltage 94, respectively is generated. Similarly, reference voltage which is different at the node during the resistance R of the circuit generating reference voltage 95, respectively is generated. Here, different reference voltage obtained by the circuit generating reference voltage 94 is called the right side reference voltage Vref (+). Different reference voltage obtained by the circuit generating reference voltage 95 is called the negative side reference voltage Vref (-).
[0194]The right side analog input voltage Vin (+) and the right side reference voltage Vref (+) are given to the capacitor C1 of each comparator 90 via the switch S15 and S16, respectively. The negative side analog input voltage Vin (-) and the negative side reference voltage Vref (-) are given to the capacitor C2 of each comparator 90 via the switch S17 and S18, respectively. The composition and operation of the comparator 90 of drawing 16 are the same as the composition of the comparator 90 of drawing 13, and operation.
[0195]Here, the difference of high potential side reference voltage VRT2 and low voltage side reference voltage VRB2 is set as $VIN_{p-p}/8$. When the switch S28 of the circuit generating reference voltage 95 and 96 and S29 are OFF, full-scale ranges are $VIN_{p-p}/16$. If the switch S28 and S29 are made one, a full-scale range will be set to $VIN_{p-p}/8$. Thus, in sub A/D converter 9b, a full-scale range can be changed 1 time and twice.
[0196]Drawing 17 is a circuit diagram of D/A converter 10 in the 2nd step of circuit 4 in the analog-to-digital circuit 1 of drawing 3. D/A converter 10 of drawing 17 is a capacity array method D/A converter.
[0197]D/A converter 10 comprises the switch S51 by the side of right [of the each plurality connected to the circuit generating reference voltage 96 which generates reference voltage, and

array form], S52 and the switch S53 of two or more negative sides, S54, two or more right side capacitors C50, and two or more negative side capacitors C51.
[0198]The circuit generating reference voltage 96 consists of the resistance R4, two or more resistance R, and the resistance R5. The resistance R4 and R5 have the resistance of the half of the resistance of the sum total of two or more resistance R. The resistance R4, two or more resistance R, and the resistance R5 are connected in series between the node N101 which receives high potential side reference voltage VRT3, and the node N102 which receives low voltage side reference voltage VRB3. The switch S30 is connected to the both ends of the resistance R4, and the switch S31 is connected to the both ends of the resistance R5.
[0199]All of the capacitor C50 and C51 have the same capacity value. From one terminal (it is hereafter called an output terminal) N111 of the capacitor C50, the differential positive side output voltage VDA (+) is generated, and the differential negative side output voltage VDA (-) is generated from one terminal (henceforth an output terminal) N112 of the capacitor C51. Each capacitor C50 and the terminal of another side of C51 are called an input terminal.
[0200]One terminal of each switch S51 is connected to the node N103 between the resistance R4 and the resistance R, and the terminal of another side is connected to the input terminal of the capacitor C50. One terminal of each switch S52 is connected to the node N104 between the resistance R5 and the resistance R, and the terminal of another side is connected to the input terminal of the capacitor C50. One terminal of each switch S53 is connected to the node N103 between the resistance R4 and the resistance R, and the terminal of another side is connected to the input terminal of the capacitor C51. One terminal of each switch S54 is connected to the node N104 between the resistance R5 and the resistance R, and the terminal of another side is connected to the input terminal of the capacitor C51.
[0201]According to the output level of the comparator 90 of sub A/D converter 9b of drawing 16, on-off control action of the switch S51, S52, S53, and S54 is carried out. The four switches S51 which receive the output signal of the same comparator 90, S52, S53, and S54 constitute 4 ream switch. For example, when the output of the one comparator 90 is high-level, and the switch S52 and S53 turn off. [the switch S51 of 4 ream switch, and S54] On the contrary, one [the switch S51 of 4 ream switch and S54 turn off, and / the switch S52 and S53] when the output of the one comparator 90 is a low level.
[0202]According to the output level of two or more comparators 90 of sub A/D converter 9b, two or more switches S51, S52, S53, and S54 carry out on-off control action, and the differential positive side output voltage VDA (+) and the differential negative side output voltage VDA (-) are obtained by the output terminal N111 and N112.
[0203]Here, the difference of high potential side reference voltage VRT3 and low voltage side reference voltage VRB3 is set as $VIN_{p-p}/4$. When the switch S30 of the circuit generating reference voltage 96 and S31 are OFF, full-scale ranges are $VIN_{p-p}/8$. If the switch S30 and S31 are made one, a full-scale range will be set to $VIN_{p-p}/4$. Thus, in D/A converter 10b, a full-scale range can be changed 1 time and twice.
[0204]Drawing 18 is a circuit diagram showing the 1st example of the composition of the subtraction amplifier 14a in the analog-to-digital circuit 1 of drawing 3.
[0205]The subtraction amplifier 14a of drawing 18 includes the operational amplifier 130, the capacity value switching circuit 131,132, the capacitor 133,134, and the switches 135-138. A switch is constituted by the MOS (metal oxide semiconductor) transistor, for example.
[0206]The capacity value switching circuit 131 is connected as feed back capacity between the inversed input terminal of the operational amplifier 130, and an inverted output terminal, and the capacity value switching circuit 132 is connected as feed back capacity between the non-inversed input terminal and the noninverting output terminal. The capacitor 133 is connected to the inversed input terminal of the operational amplifier 130 as input capacitance, and the capacitor 134 is connected to the non-inversed input terminal as input capacitance.
[0207]The differential positive side output voltage VDA (+) outputted from the right side analog output voltage Vo (+) and D/A converter 10b which are outputted is given to the capacitor 133 via the switch 135,136, respectively from the arithmetic amplifier 11 of drawing 3. The differential

positive side output voltage VDA (−) outputted from the negative side analog output voltage Vo (−) and D/A converter 10b which are outputted is given to the capacitor 134 via the switch 137,138, respectively from the arithmetic amplifier 11. The inversed input terminal, the inverted output terminal, non-inversed input terminal, and noninverting output terminal of the operational amplifier 130 are grounded via the switch 139,140,141,142, respectively.

[0208]Operation of the subtraction amplifier 14a of drawing 18 is the same as operation of the arithmetic amplifier 11a of drawing 4. The right side analog input voltage Vin (+) and the negative side analog input voltage Vin (−) which are given in the circuit 4 of the next step are obtained from the inverted output terminal and noninverting output terminal of the operational amplifier 130.

[0209]Here, the profit of the subtraction amplifier 14a can be changed by changing the capacity value of the capacity value switching circuit 131,132.

[0210]Drawing 19 is a circuit diagram showing the 2nd example of the composition of the subtraction amplifier 14a in the analog-to-digital circuit 1 of drawing 3.

[0211]The subtraction amplifier 14a of drawing 19 includes the operational amplifier 130, the capacitor 139,140, the capacity value switching circuit 141,142, and the switches 135-140.

[0212]The capacitor 139 is connected as feed back capacity between the inversed input terminal of the operational amplifier 130, and an inverted output terminal, and the capacitor 140 is connected as feed back capacity between the non-inversed input terminal and the noninverting output terminal. The capacity value switching circuit 141 is connected to the inversed input terminal of the operational amplifier 130 as input capacitance, and the capacity value switching circuit 142 is connected to the non-inversed input terminal as input capacitance.

[0213]The differential positive side output voltage VDA (+) outputted from the right side analog output voltage Vo (+) and D/A converter 10b which are outputted is given to the capacity value switching circuit 141 via the switch 135,136, respectively from the arithmetic amplifier 11 of drawing 3. The differential positive side output voltage VDA (−) outputted from the negative side analog output voltage Vo (−) and D/A converter 10b which are outputted is given to the capacity value switching circuit 142 via the switch 137,138, respectively from the arithmetic amplifier 11. The inversed input terminal, the inverted output terminal, non-inversed input terminal, and noninverting output terminal of the operational amplifier 130 are grounded via the switch 139,140,141,142, respectively.

[0214]Operation of the subtraction amplifier 14a of drawing 19 is the same as operation of the arithmetic amplifier 11a of drawing 5. The right side analog input voltage Vin (+) and the negative side analog input voltage Vin (−) which are given in the circuit 4 of the next step are obtained from the inverted output terminal and noninverting output terminal of the operational amplifier 130.

[0215]Here, the profit of the subtraction amplifier 14a can be changed by changing the capacity value of the capacity value switching circuit 141,142.

[0216]The switch Sa of the above-mentioned embodiment, S1a, S2a, S24, S25, S26, S28, S29, S30, and S31 are formed, for example of an MOS (metal oxide semiconductor) field effect transistor.

[0217]According to the above-mentioned embodiment, the switch Sa, S1a, S2a, S24, S25, S26, S28, S29, S30, and S31 are used as a switch part of a switching means. In this case, the switch Sa, S1a, S2a, S24, S25, S26, S28, S29, S30, and S31 can be changed to one or OFF at the time of manufacture or use. The switch part of a switching means is not limited to a switch. For example, the fuse which can be blown out with laser may be used as a switch part, and the mask switch part for patterning of top layer metal may be used as a switch part.

[0218]Drawing 20 is a circuit diagram showing other examples of a switch part. In the example of drawing 20, the fuse Fa is used instead of the switch Sa of the arithmetic amplifier 11a of drawing 6. The fuse Fa can consist of polysilicon, for example, and can be blown out with laser. At the time of manufacture, the profit of the arithmetic amplifier 11a can be changed by whether laser is used and the fuse Fa is blown out.

[0219]Drawing 21 and drawing 22 are the figures showing the example of further others of a switch part, show a top view to the upper part and show a sectional view to the lower part.

[0220]In the capacity formation section C500, the electrode 501,502 of the capacitor is formed of lower layer metal LM1 and LM2. The electrode 507,508 is formed of lower layer metal LM1. With the top layer metal UM, the electrode 512,513 is formed with a prescribed interval, and the electrode 514,515 is formed with the prescribed interval. The electrode 501 is connected to the electrode 512 via the metal in the through hole 503, and the electrode 502 is connected to the electrode 514 via the metal in the through hole 504. The electrode 507 is connected to the electrode 512 via the metal in the through hole 505, and the electrode 508 is connected to the electrode 515 via the metal in the through hole 506.
[0221]For example, 507 is connected to the inversed input terminal of the operational amplifier 110 of drawing 6, and the electrode 508 is connected to the inverted output terminal of the operational amplifier 110 of drawing 6.
[0222]The capacity formation section C500 is formed of the electrode 501,502, and mask switch part municipal solid waste is formed between the electrodes 512,513 and of between the electrodes 514,515, respectively. The capacity formation block C500 is equivalent to capacitor Ca of drawing 6, for example.
[0223]At the time of manufacture, between the electrodes 512,513 and between the electrodes 514,515 can be changed to a connected state and a cut off state by changing the pattern of the mask arranged on mask switch part municipal solid waste.
[0224]As shown in drawing 21, between the electrodes 512,513 and between the electrodes 514,515 are connectable by using the mask that the metal layer 510,511 is formed with the top layer metal UM between the electrodes 512,513 and between the electrodes 514,515.
[0225]As shown in drawing 22, between the electrodes 512,513 and between the electrodes 514,515 can be intercepted by using the mask that a metal layer is not formed with the top layer metal UM between the electrodes 512,513 and between the electrodes 514,515.
[0226]In the example of drawing 21 and drawing 22, the capacity formation section C500 is thoroughly separable from an operational amplifier by providing a mask switch part in the terminal of both capacity formation sections C500, respectively.
[0227]In the circuit of the stages with an arbitrary analog-to-digital circuit in which this invention is not limited to the above-mentioned embodiment, At least one of the D/A converters which have an arithmetic amplifier which has a switchable profit, a subtraction amplifier which has a switchable profit, a sub A/D converter which has a switchable full-scale range, and a switchable full-scale range may be used.

[Translation done.]

* NOTICES *

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TECHNICAL FIELD

[Field of the Invention]This invention relates to the analog-to-digital circuit which has multi stage pipeline (step flash plate) composition.

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PRIOR ART

[Description of the Prior Art]In recent years, the demand of the analog-to-digital circuits for video signal processing (A/D converter) is large with progress of the digital processing art of a video signal. Since fast conversion operation was required of the analog-to-digital circuit for video signal processing, 2 step flash plate (parallel two steps) method was used widely conventionally.
[0003]However, since conversion precision sufficient by 2 step flash plate method was no longer acquired with increase of the conversion number of bits, the analog-to-digital circuit which has multi stage pipeline (step flash plate) composition was developed.
[0004]Drawing 23 is a block diagram showing the conventional analog-to-digital circuit indicated by JP,11-88172,A. The analog-to-digital circuit 100 of drawing 23 has 10-bit four-step pipeline constitution.
[0005]In drawing 23, the analog-to-digital circuit 100 comprises the circuits 3-6, two or more latch circuitry 7, and the output circuit 8 of the 2 or 1st step - the 4th step of sample hold circuit.
[0006]The 1st (first rank) step - the 3rd step of circuits 3, 4, and 5 are provided with sub A/D converter 9, D/A converter 10, the arithmetic amplifier 11, the subtractor circuit 12, and the arithmetic amplifier 13. The subtractor circuit 12 and the arithmetic amplifier 13 constitute the subtraction amplifier 14. The profit of the arithmetic amplifier 11 in the 1st step of circuit 3 is 1, and the profit of the arithmetic amplifiers 11 and 13 in the arithmetic amplifier 13 in the 1st step of circuit 3, the 2nd step, and the 3rd step of circuit 4 and 5 is 2. The 4th (final stage) step of circuit 6 is provided only with sub A/D converter 9.
[0007]4 bit configurations and the 2-4th step of circuits 4-6 of the 1st step of circuit 3 are 2 bit configurations, respectively. Similarly in the 1-3rd step of circuits 3-5, the number of bits (bit configuration) of sub A/D converter 9 and D/A converter 10 is set up.

[Translation done.]

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EFFECT OF THE INVENTION

[The means for solving a technical problem and an effect of the invention] (1) The analog-to-digital circuit concerning the 1st invention invention of the 1st, Have the multi stage pipeline constitution which consists of two or more steps of circuits, and the circuit of each stage except the circuit of a final stage, The analog-digital converter which changes the inputted analog signal into a digital signal, The digital-to-analog converter which changes into an analog signal the digital signal outputted from an analog-digital converter, Have the 1st arithmetic amplifier that amplifies the difference of the analog signal inputted and the analog signal outputted from a digital-to-analog converter, and the circuit of a final stage, The analog-digital converter which changes the inputted analog signal into a digital signal is included, The analog-digital converter which has a switching means from which at least one step of circuit except the circuit of a final stage changes a full-scale range to two or more steps, At least one of the 1st arithmetic amplifiers that have a switching means which changes the digital-to-analog converter and profit which have a switching means which changes a full-scale range to two or more steps to two or more steps is included, And/or, the circuit of a final stage contains the analog-digital converter which has a switching means which changes a full-scale range to two or more steps.
[0045]In an analog-to-digital circuit concerning this invention, An analog-digital converter which has a switching means from which at least one step of circuit except a circuit of a final stage changes a full-scale range to two or more steps, At least one of the 1st arithmetic amplifiers that have a switching means which changes a digital-to-analog converter and a profit which have a switching means which changes a full-scale range to two or more steps, and to change to two or more steps is included, And/or, since a circuit of a final stage contains an analog-digital converter which has a switching means which changes a full-scale range to two or more steps, At least one of a full-scale range of an analog-to-digital circuit, a full-scale range of a digital-to-analog converter, and profits of the 1st arithmetic amplifier can be changed.
[0046]Redesign of circuitry becomes unnecessary even if a voltage range of an analog input signal is changed by that cause by changing a differential double end input method into a single-ended input method. Redesign of circuitry becomes unnecessary, when changing a voltage range of an analog input signal of a single-ended input, or also when changing a voltage range of an analog input signal of a differential double end input.
[0047]Therefore, an input method between change of a voltage range of an analog input signal or a differential double end input, and a single-ended input can be changed easily, without redesigning circuitry.
[0048]As a result, while being able to attain shortening of a development cycle of an analog-to-digital circuit, low power consumption can be easily performed by optimizing optimization of a voltage range.
[0049](2) An analog-to-digital circuit concerning the 2nd invention invention of the 2nd, In composition of an analog-to-digital circuit concerning the 1st invention, a circuit of each stage except a circuit of a final stage, The 2nd arithmetic amplifier of at least one step of circuit except a circuit of a final stage has a switching means which changes a profit to two or more steps, including further the 2nd arithmetic amplifier that amplifies an inputted analog signal and is given to the 1st arithmetic amplifier.

[0050]In this case, by changing a profit of the 2nd arithmetic amplifier of at least one step of circuit to two or more steps, It becomes possible to change an input method between change of a voltage range of an analog input signal or a differential double end input, and a single-ended input easily, without redesigning circuitry.
[0051](3) In composition of an analog-to-digital circuit which an analog-to-digital circuit concerning the 3rd invention invention of the 3rd requires for the 1st or 2nd invention, the 1st arithmetic amplifier of at least one step of circuit except a circuit of a final stage has a switching means which changes a profit to two or more steps.
[0052]In this case, by changing a profit of the 1st arithmetic amplifier of at least one step of circuit to two or more steps, It becomes possible to change an input method between change of a voltage range of an analog input signal or a differential double end input, and a single-ended input easily, without redesigning circuitry.
[0053](4) An analog-to-digital circuit concerning the 4th invention invention of the 4th, In composition of an analog-to-digital circuit concerning the 1st - the 3rd one of inventions, an analog-digital converter of at least one step of circuit has a switching means which changes a full-scale range to two or more steps.
[0054]In this case, a full-scale range of an analog-digital converter of at least one step of circuit to two or more steps by switchable ******. It becomes possible to change an input method between change of a voltage range of an analog input signal or a differential double end input, and a single-ended input easily, without redesigning circuitry.
[0055](5) An analog-to-digital circuit concerning the 5th invention invention of the 5th, In composition of an analog-to-digital circuit concerning the 1st - the 4th one of inventions, a digital-to-analog converter of at least one step of circuit except a circuit of a final stage has a switching means which changes a full-scale range to two or more steps.
[0056]In this case, by changing a full-scale range of a digital-to-analog converter of at least one step of circuit to two or more steps, It becomes possible to change an input method between change of a voltage range of an analog input signal or a differential double end input, and a single-ended input easily, without redesigning circuitry.
[0057](6) An analog-to-digital circuit concerning the 6th invention invention of the 6th, In composition of an analog-to-digital circuit concerning the 2nd invention, the 2nd arithmetic amplifier of at least one step of circuit, It has input capacitance, feedback capacity, and an operational amplifier, an inputted analog signal is amplified on a profit which becomes settled with a value of input capacitance, and a value of feedback capacity, and a switching means contains a variable region which sets either [at least] a value of input capacitance, or a value of feedback capacity as variable.
[0058]In this case, an inputted analog signal is amplified on a profit which becomes settled with a value of input capacitance, and a value of feedback capacity. Therefore, a profit of the 2nd arithmetic amplifier can be easily changed by changing either [at least] a value of input capacitance of an operational amplifier, or a value of feedback capacity.
[0059](7) In composition of an analog-to-digital circuit which requires an analog-to-digital circuit concerning invention the 7th invention of the 7th for the 6th invention, a variable region contains a switch part changed to a state or the state where it connected too hastily where a part of input capacitance or feedback capacity was separated.
[0060]In this case, input capacitance or feedback capacity of an operational amplifier can be changed by changing to a state or the state where it connected too hastily where a part of input capacitance or feedback capacity was separated by switch part. Thereby, a profit of the 2nd arithmetic amplifier can be changed easily.
[0061](8) An analog-to-digital circuit concerning the 8th invention invention of the 8th, In composition of an analog-to-digital circuit concerning the 3rd invention, the 1st arithmetic amplifier of at least one step of circuit, It has input capacitance, feedback capacity, and an operational amplifier, an inputted analog signal is amplified on a profit which becomes settled with a value of input capacitance, and a value of feedback capacity, and a switching means contains a variable region which sets either [at least] a value of input capacitance, or a value of feedback capacity as variable.

[0062]In this case, an inputted analog signal is amplified on a profit which becomes settled with a value of input capacitance, and a value of feedback capacity. Therefore, a profit of the 1st arithmetic amplifier can be easily changed by changing either [at least] a value of input capacitance of an operational amplifier, or a value of feedback capacity.
[0063](9) In composition of an analog-to-digital circuit which requires an analog-to-digital circuit concerning invention the 9th invention of the 9th for the 8th invention, a variable region contains a switch part changed to a state or the state where it connected too hastily where a part of input capacitance or feedback capacity was separated.
[0064]In this case, input capacitance or feedback capacity of an operational amplifier can be changed from changing to a state or the state where it connected too hastily where a part of input capacitance or feedback capacity was separated by switch part. Thereby, a profit of the 1st arithmetic amplifier can be changed easily.
[0065](10) An analog-to-digital circuit concerning the 10th invention invention of the 10th, In composition of an analog-to-digital circuit concerning the 9th invention, a switch part is connected to the 2nd capacity in series or in parallel including the 1st and 2nd capacity by which feedback capacity was provided in parallel or in series between an input terminal of an operational amplifier, and an output terminal.
[0066]If a switch part is made into a connected state, the 1st and 2nd capacity will be connected in parallel or in series between an input terminal of an operational amplifier, and an output terminal. Thereby, feedback capacity increases or decreases. If a switch part is made into a cut off state, only the 1st capacity will be connected between an input terminal of an operational amplifier, and an output terminal. Thereby, feedback capacity decreases or increases.

[0067](11) A switch part is connected to an output terminal of an operational amplifier in composition of an analog-to-digital circuit which requires an analog-to-digital circuit concerning invention the 11th invention of the 11th for the 10th invention.
[0068]When the 2nd capacity is connected to an output side rather than a switch part, even if a switch part is set as a cut off state, parasitic capacitance of the 2nd capacity is charged. By that cause, it will be necessary to take parasitic capacitance into consideration, and a profit will vary with dispersion in parasitic capacitance at the time of setting out of a profit. Here, by connecting a switch part to an output side rather than the 2nd capacity, when a switch part is set as a cut off state, the 2nd capacity is separated from an output terminal by switch part with parasitic capacitance. Therefore, it becomes unnecessary to take parasitic capacitance of the 2nd capacity into consideration at the time of setting out of a profit, and dispersion in a profit by dispersion in parasitic capacitance is lost.
[0069](12) In composition of an analog-to-digital circuit which requires an analog-to-digital circuit concerning invention the 12th invention of the 12th for the 9th invention, input capacitance is provided in an input terminal of an operational amplifier in parallel or in series.
[0070]If a switch part is made into a connected state, the 1st and 2nd capacity will be connected to an input terminal of an operational amplifier in parallel or in series. Thereby, input capacitance increases or decreases. Only the 1st capacity will be connected to an input terminal of an operational amplifier if a switch part is made into a cut off state. Thereby, input capacitance decreases or increases.
[0071](13) A switch part is connected to an input side of the 2nd capacity in composition of an analog-to-digital circuit which requires an analog-to-digital circuit concerning invention the 13th invention of the 13th for the 12th invention.
[0072]When the 2nd capacity is connected to an input side rather than a switch part, even if a switch part is set as a cut off state, parasitic capacitance of the 2nd capacity is charged. By that cause, it will be necessary to take parasitic capacitance into consideration, and a profit will vary with dispersion in parasitic capacitance at the time of setting out of a profit. Here, by connecting a switch part to an input side rather than the 2nd capacity, when a switch part is set as a cut off state, it is separated from a node in which the 2nd capacity receives an input signal by a switch part with parasitic capacitance. Therefore, it becomes unnecessary to take parasitic capacitance of the 2nd capacity into consideration at the time of setting out of a profit, and

dispersion in a profit by dispersion in parasitic capacitance is lost.
[0073](14) An analog-to-digital circuit concerning the 14th invention invention of the 14th, In composition of an analog-to-digital circuit concerning the 4th invention, an analog-digital converter of at least one step of circuit, A switching means contains a variable region which sets as variable two or more reference voltage generated by circuit generating reference voltage including circuit generating reference voltage which generates two or more reference voltage, and two or more comparators compared with an analog signal into which two or more reference voltage generated by circuit generating reference voltage was inputted.
[0074]In this case, a voltage range of reference voltage can be changed by changing reference voltage generated by circuit generating reference voltage. Thereby, a full-scale range of an analog-digital converter can be changed easily.
[0075](15) An analog-to-digital circuit concerning the 15th invention invention of the 15th, In composition of an analog-to-digital circuit concerning the 5th invention, a digital-to-analog converter of at least one step of circuit except a circuit of a final stage, Circuit generating reference voltage which generates reference voltage, and two or more capacity connected to a common terminal, Two or more switches which give reference voltage which was connected between circuit generating reference voltage and two or more capacity, and was generated by circuit generating reference voltage according to a digital signal inputted to two or more capacity, respectively are included, A switching means contains a variable region which sets reference voltage generated by circuit generating reference voltage as variable.
[0076]In this case, a voltage range of reference voltage can be changed by changing reference voltage generated by circuit generating reference voltage. Thereby, a full-scale range of a digital-to-analog converter can be changed easily.
[0077]
[Embodiment of the Invention](1) The 1st embodiment drawing 1 is a block diagram showing the composition of the pipeline type analog-to-digital circuit in a 1st embodiment of this invention. The analog-to-digital circuit of drawing 1 has 10-bit four-step pipeline constitution.
[0078]In drawing 1, the analog-to-digital circuit 1 comprises the circuits 3-6, two or more latch circuitry 7, and the output circuit 8 of the 2 or 1st step - the 4th step of sample hold circuit.
[0079]The 1st (first rank) step of circuit 3 is provided with the arithmetic amplifier 11a, the subtractor circuit 12, and the arithmetic amplifier 13 which have sub A/D converter 9a which has a switchable full-scale range, D/A converter 10, and a switchable profit. The subtractor circuit 12 and the arithmetic amplifier 13 constitute the subtraction amplifier 14. The 2nd step and the 3rd step of circuits 4 and 5 are provided with sub A/D converter 9, D/A converter 10, the arithmetic amplifier 11, the subtractor circuit 12, and the arithmetic amplifier 13. The subtractor circuit 12 and the arithmetic amplifier 13 constitute the subtraction amplifier 14. The 4th (final stage) step of circuit 6 is provided only with sub A/D converter 9.
[0080]That the pipeline type analog-to-digital circuit 1 of drawing 1 differs from the conventional analog-to-digital circuit 100 of drawing 20, It is the point that the arithmetic amplifier 11a which has sub A/D converter 9a and the switchable profit which have a switchable full-scale range is used for the 1st step of circuit 3.
[0081]Here, the full-scale range of sub A/D converter 9 in the 1st step of circuit 3, It changes to voltage range VIN_{p-p} equal to it when the voltage range of an analog input signal is VIN_{p-p}, and when the voltage ranges of an analog input signal are $VIN_{p-p}/2$, it changes to voltage range $VIN_{p-p}/2$. [equal to it] The profit of the arithmetic amplifier 11a in the 1st step of circuit 3 is changed 1 time, when the voltage range of an analog input signal is VIN_{p-p}, and when the voltage ranges of an analog input signal are $VIN_{p-p}/2$, it is changed twice.
[0082]The full-scale range of D/A converter 10 in the 1st step - the 3rd step of circuit 3-5 is fixed, and the full-scale range of sub A/D converter 9 in the 2nd step - the 4th step of circuit 4-6 is being fixed. The profit of the arithmetic amplifiers 11 and 13 in the arithmetic amplifier 13 in the 1st step of circuit 3, the 2nd step, and the 3rd step of circuit 3 and 4 is 2.
[0083]4 bit configurations and the 2-4th step of circuits 4-6 of the 1st step of circuit 3 are 2 bit

configurations, respectively. Similarly in the 1-3rd step of circuits 3-5, the number of bits (bit configuration) of sub A/D converters 9 and 9a and D/A converter 10 is set up.
[0084]Operation of the analog-to-digital circuit 1 of drawing 1 in case the voltage range of an analog input signal is VIN_{p-p}, and the voltage range of each part are the same as that of the analog-to-digital circuit 100 of drawing 20.
[0085]Here, operation of the analog-to-digital circuit 1 of drawing 1 in case the voltage ranges of an analog input signal are $VIN_{p-p}/2$, and the output voltage range of each part are explained.
[0086]The sample hold circuit 2 samples the analog input signal Vin, and carries out fixed time maintenance. The analog input signal Vin outputted from the sample hold circuit 2 is transmitted to the 1st step of circuit 3.
[0087]In the 1st step of circuit 3, sub A/D converter 9a performs an analog to digital to the analog input signal Vin of voltage range $VIN_{p-p}/2$. The full-scale range of sub A/D converter 9a at this time is changed to $VIN_{p-p}/2$ as mentioned above.
[0088]Top 4-bit digital output (2^9, 2^8, 2^7, 2^6) which is an A/D conversion result of sub A/D converter 9a is transmitted to the output circuit 8 via the four latch circuitry 7 while it is transmitted to D/A converter 10. D/A converter 10 changes into an analog signal top 4-bit digital output which is an A/D conversion result of sub A/D converter 9a.
[0089]Since the full-scale range of D/A converter 10 is being fixed to VIN_{p-p}, the normal output voltage range of D/A converter 10 is expressed like a following formula.
[0090]
(The 1st step of resolution-1) x(full-scale range of D/A converter 10)/(the 1st step of resolution)
$= (2^4-1) \times (VIN_{p-p}) / 2^4 = 15VIN_{p-p}/16$ one side and the arithmetic amplifier 11a sample the analog input signal Vin, and amplify and hold it. As mentioned above, since a profit is changed twice when the voltage ranges of an analog input signal are $VIN_{p-p}/2$, the output voltage range of the arithmetic amplifier 11a is expressed like a following formula.
[0091]
(Voltage range of the analog input signal Vin) x (profit of the arithmetic amplifier 11a)
$= (VIN_{p-p}/2)$ The x2 $= VIN_{p-p}$ subtraction amplifier 14 subtracts and amplifies the analog input signal Vin and the D/A conversion result of D/A converter 10 which were outputted from the arithmetic amplifier 11a. The output of the subtraction amplifier 14 is transmitted to the 2nd step of circuit 4.
[0092]The output voltage range of the 1st step of subtraction amplifier 14 is expressed like a following formula.
(Output voltage range of the arithmetic amplifier 11a) x (- (normal output voltage range of D/A converter 10)) (profit of the subtraction amplifier 14)
$= (VIN_{p-p}) (- (15VIN_{p-p}/16))$ In the x2 $= VIN_{p-p}/82$ step circuit 4, sub A/D converter 9 performs an A/D conversion to the output of the subtraction amplifier 14 of the 1st step of circuit 3. The A/D conversion result of sub A/D converter 9 is transmitted to the output circuit 8 via the three latch circuitry 7 while it is transmitted to D/A converter 10. Thereby, a 2-bit digital output (2^5, 2^4) is obtained at least for Nakagami from the 2nd step of circuit 4.
[0093]On the other hand, the arithmetic amplifier 11 amplifies the output of the subtraction amplifier 14 of the 1st step of circuit 3. The subtraction amplifier 14 subtracts and amplifies the output of the arithmetic amplifier 11, and the D/A conversion result of D/A converter 10. The output of the subtraction amplifier 14 is transmitted to the 3rd step of circuit 5.
[0094]In the 3rd step of circuit 5, the same operation as the 2nd step of circuit 4 is performed to the output of the subtraction amplifier 14 of the 2nd step of circuit 4. Thereby, a 2-bit digital output (2^3, 2^2) is obtained at least for Nakashita from the 3rd step of circuit 5.
[0095]In the 4th step of circuit 6, sub A/D converter 9 performs an A/D conversion to the output of the subtraction amplifier 14 of the 3rd step of circuit 5, and the digital output (2^1, 2^0)

of 2 bits of low ranks is obtained.
[0096]The digital output of the 1st step – the 4th step of circuits 3–6 arrives at the output circuit 8 simultaneously through each latch circuitry 7. That is, each latch circuitry 7 is formed in order to take the synchronization of the digital output of each circuits 3–6.
[0097]The output circuit 8 carries out the after [a digital compensation process] parallel output of the 10–bit digital output Dout of the analog input signal Vin, when required.
[0098]As mentioned above, when the voltage ranges of an analog input signal are $VIN_{p-p}/2$. By changing the full–scale range of the profit of the arithmetic amplifier 11a of the 1st step of circuit 3, and sub A/D converter 9a of the 1st step of circuit 3, The voltage range of the output signal given in the 2nd step of circuit 5 is set to $VIN_{p-p}/8$ from the subtraction amplifier 14 of the 1st step of circuit 3 like the case where the voltage range of an analog input signal is VIN_{p-p}. Thereby, although the voltage range of the analog input signal Vin became half, the digital output same before the voltage range of an analog input signal becomes half is obtained.
[0099]Therefore, the analog–to–digital circuit corresponding to change of the voltage range of an analog input signal can be provided, without changing a circuit design.
[0100]According to this embodiment, the analog–to–digital circuit of a differential double end input method can be changed into the analog–to–digital circuit of a single–ended input method, without changing circuitry.
[0101]Drawing 2 (a) and (b) is a figure showing setting out in the case of changing the analog–to–digital circuit 1 of drawing 1 to a differential double end input method and a single–ended input method, respectively.
[0102]As shown in drawing 2 (a), at the time of a differential double end input, the profit of the arithmetic amplifier 11a is changed 1 time, and the full–scale range of sub A/D converter 9a is changed to $2VIN_{p-p}$. In this example, the right side analog input voltage Vin of the analog input signal Vin of a differential double end input (+) changes in 1.0V to 2.0V, and the negative side analog input voltage Vin (–) changes from 2.0V in 1.0V. The voltage range of the analog input signal Vin becomes like a following formula.
[0103]The maximum of $2VIN_{p-p}$= {Vin(+)–Vin (–)} – minimum =2.0 [V] of {Vin(+)–Vin (–)}
In this case, the right side reference voltage Vref of sub A/D converter 9a (+) changes in 1.0V to 2.0V, and the negative side reference voltage Vref (–) changes from 2.0V in 1.0V.
[0104]As shown in drawing 2 (b), at the time of a single–ended input, the profit of the arithmetic amplifier 11a is changed twice, and the full–scale range of sub A/D converter 9a is changed to VIN_{p-p}. The right side analog input voltage Vin of the analog input signal Vin of the single–ended input in this example (+) changes in 1.0V to 2.0V, and that of the negative side analog input voltage Vin (–) is constant 1.5V. The voltage range of the analog input signal Vin becomes like a following formula.
[0105]The maximum of VIN_{p-p}= {Vin(+)–Vin (–)} – minimum =1.0 [V] of {Vin(+)–Vin (–)}
In this case, the right side reference voltage Vref of sub A/D converter 9a (+) changes in 1.0V to 2.0V, and its negative side reference voltage Vref (–) is constant 1.5V.
[0106]Thus, in the analog–to–digital circuit 1 of drawing 1, even if the voltage range of an analog input signal is set to one half by changing a differential double end input method into a single–ended input method, redesign of circuitry becomes unnecessary.
[0107]Redesign of circuitry becomes unnecessary, when changing the voltage range of the analog input signal of a single–ended input into one half, and also when changing the voltage range of the analog input signal of a differential double end input into one half.
[0108]Thus, in the same LSI (large scale integration circuit), the voltage range of the output of an analog input signal and an arithmetic amplifier, the output of a D/A conversion circuit, and the output of a subtraction amplifier can be changed programmably. As a result, while being able to attain shortening of a development cycle, it is also possible to perform low power consumption.
[0109](2) The 2nd embodiment drawing 3 is a block diagram showing the composition of the pipeline type analog–to–digital circuit in a 2nd embodiment of this invention. The analog–to–

digital circuit 1 of drawing 3 also has 10-bit four-step pipeline constitution.
[0110]In drawing 3, the analog-to-digital circuit 1 comprises the circuits 3-6, two or more latch circuitry 7, and the output circuit 8 of the 2 or 1st step - the 4th step of sample hold circuit.
[0111]4 bit configurations and the 2-4th step of circuits 4-6 of the 1st step of circuit 3 are 2 bit configurations, respectively. Similarly in the 1-3rd step of circuits 3-5, the number of bits (bit configuration) of sub A/D converters 9 and 9b and D/A converters 10 and 10b is set up.
[0112]The 1st (first rank) step of circuit 3 is provided with the arithmetic amplifier 13a which has sub A/D converter 9, D/A converter 10, the arithmetic amplifier 11, the subtractor circuit 12, and a switchable profit. The subtractor circuit 12 and the arithmetic amplifier 13a constitute the subtraction amplifier 14a.
[0113]The 2nd step and the 3rd step of circuits 4 and 5 are provided with sub A/D converter 9b which has a switchable full-scale range, D/A converter 10b which has a switchable full-scale range, the arithmetic amplifier 11, the subtractor circuit 12, and the arithmetic amplifier 13. The subtractor circuit 12 and the arithmetic amplifier 13 constitute the subtraction amplifier 14. The 4th (final stage) step of circuit 6 is provided only with sub A/D converter 9b which has a switchable full-scale range.
[0114]Here, the 2nd step - the 4th step of sub A/D converter 9b shall have the 2nd step - the 4th step of A/D converter 9 of drawing 20 twice the accuracy of sub. Redesign of the analog-to-digital circuit 1 at the time of using for the 2nd step - the 4th step hereafter sub A/D converter 9b which has twice as many accuracy as this is explained.
[0115]It is switchable 1 time and twice in the profit of the subtraction amplifier 14a in the 1st step of circuit 3. It is switchable to $VIN_{p-p}/8$, and $VIN_{p-p}/16$ in the full-scale range of sub A/D converter 9b in the 2nd step - the 4th step of circuit 4-6. It is switchable to $VIN_{p-p}/4$, and $VIN_{p-p}/8$ in the full-scale range of D/A converter 10b in the 2nd step and the 3rd step of circuit 4 and 5.
[0116]Here, the profit of the subtraction amplifier 14a in the 1st step of circuit 3 is changed 1 time. The full-scale range of sub A/D converter 9b in the 2nd step - the 4th step of circuit 4-6 is changed to $VIN_{p-p}/16$, and the full-scale range of D/A converter 10b in the 2nd step and the 3rd step of circuit 4 and 5 is changed to $VIN_{p-p}/8$. The full-scale range of sub A/D converter 9 in the 1st step of circuit 3 is VIN_{p-p}. The profit of the arithmetic amplifiers 11 and 13 in the 2nd step and the 3rd step of circuit 3 and 4 is 2.
[0117]Here, operation of the analog-to-digital circuit 1 of drawing 1 in case the voltage range of an analog input signal is VIN_{p-p}, and the output voltage range of each part are explained.
[0118]The sample hold circuit 2 samples the analog input signal Vin, and carries out fixed time maintenance. The analog input signal Vin outputted from the sample hold circuit 2 is transmitted to the 1st step of circuit 3.
[0119]In the 1st step of circuit 3, sub A/D converter 9 performs an analog to digital to the analog input signal Vin of voltage range VIN_{p-p}. The full-scale range of sub A/D converter 9 at this time is VIN_{p-p}.
[0120]Top 4-bit digital output (2^9, 2^8, 2^7, 2^6) which is an A/D conversion result of sub A/D converter 9 is transmitted to the output circuit 8 via the four latch circuitry 7 while it is transmitted to D/A converter 10. D/A converter 10 changes into an analog signal top 4-bit digital output which is an A/D conversion result of sub A/D converter 9.
[0121]Since the full-scale range of D/A converter 10 is being fixed, the normal output voltage range of D/A converter 10 is expressed like a following formula.
[0122]
(The 1st step of resolution-1) x(full-scale range of D/A converter 10)/(the 1st step of resolution)
$= (2^4-1) \times (VIN_{p-p}) / 2^4 = 15VIN_{p-p}/16$ one side and the arithmetic amplifier 11 sample the analog input signal Vin, and amplify and hold it. Since the profit of the arithmetic amplifier 11 is 1

time, the output voltage range of the arithmetic amplifier 11 is expressed like a following formula.

[0123]
(Voltage range of the analog input signal Vin) x (profit of the arithmetic amplifier 11)
= The $VIN_{p-p}x1 = VIN_{p-p}$ subtraction amplifier 14a subtracts and amplifies the analog input signal Vin and the D/A conversion result of D/A converter 10 which were outputted from the arithmetic amplifier 11. The output of the subtraction amplifier 14a is transmitted to the 2nd step of circuit 4.
[0124]Since the profit of the 1st step of subtraction amplifier 14a is changed to 1, the output voltage range of the 1st step of subtraction amplifier 14a is expressed like a following formula.
[0125]
(Output voltage range of the arithmetic amplifier 11) x (- (normal output voltage range of D/A converter 10)) (profit of the subtraction amplifier 14a)
$= (VIN_{p-p})$ $(- (15VIN_{p-p}/16))$ In the $x1 = VIN_{p-p}/162$ step circuit 4, sub A/D converter 9b performs an A/D conversion to the output of the subtraction amplifier 14a of the 1st step of circuit 3. The A/D conversion result of sub A/D converter 9b is transmitted to the output circuit 8 via the three latch circuitry 7 while it is transmitted to D/A converter 10b.
[0126]In this case, since sub A/D converter 9b has A/D converter 9 of drawing 20 twice the accuracy of sub, A 2-bit digital output (2^5, 2^4) is obtained at least for Nakagami from the 2nd step of circuit 4 by full-scale range $VIN_{p-p}/16$ of the half of sub A/D converter 9 of drawing 20.
[0127]At least Nakagami whose D/A converter 10b is an A/D conversion result of sub A/D converter 9b changes a 2-bit digital output into an analog signal.
[0128]Since the full-scale range of D/A converter 10b is changed to $VIN_{p-p}/8$ of the half of D/A converter 10 of drawing 20, the normal output voltage range of D/A converter 10b is expressed like a following formula.
[0129]
(The 2nd step of resolution-1) x (full-scale range of D/A converter 10b)
/(the 2nd step of resolution)
$= (2^2-1) \times (VIN_{p-p}/8) / 2^2 = 3VIN_{p-p}/32$ one side and the arithmetic amplifier 11 amplify the output of the subtraction amplifier 14a of the 1st step of circuit 3. As mentioned above, since the profit of the subtraction amplifier 14a of the 1st step of circuit 3 is changed to 1, the output voltage range of the arithmetic amplifier 11a is expressed like a following formula.
[0130]
(Output voltage range of the 1st step of subtraction amplifier 14a) x (profit of the arithmetic amplifier 11)
$= (VIN_{p-p}/16)$ The $x2 = VIN_{p-p}/8$ subtraction amplifier 14 subtracts and amplifies the output of the arithmetic amplifier 11, and the D/A conversion result of D/A converter 10b. The output of the subtraction amplifier 14 is transmitted to the 3rd step of circuit 5.
[0131]The output voltage range of the 2nd step of subtraction amplifier 14 is expressed like a following formula.
(Output voltage range of the arithmetic amplifier 11) x (- (normal output voltage range of D/A converter 10b)) (profit of the subtraction amplifier 14)
$= (VIN_{p-p}/8)$ $(- (3VIN_{p-p}/32))$ In the $x2 = VIN_{p-p}/16$ 3 step circuit 5, the same operation as the 2nd step of circuit 4 is performed to the output of the subtraction amplifier 14 of the 2nd step of circuit 4. In this case, since sub A/D converter 9b has A/D converter 9 of drawing 20 twice the accuracy of sub, A 2-bit digital output (2^3, 2^2) is obtained at least for Nakashita from the 3rd step of circuit 5 by full-scale range $VIN_{p-p}/16$ of the half of sub A/D converter 9 of drawing 20.
The output voltage range of each part is the same as that of the 2nd step of circuit 4.
[0132]In the 4th step of circuit 6, sub A/D converter 9b performs an A/D conversion to the output of the subtraction amplifier 14 of the 3rd step of circuit 5. In this case, since sub A/D

converter 9b has A/D converter 9 of drawing 20 twice the accuracy of sub, The digital output (2 ^{1}, 2 ^{0}) of 2 bits of low ranks is obtained from the 4th step of circuit 6 by full-scale range VIN_{p-p}/16 of the half of sub A/D converter 9 of drawing 20.

[0133]The digital output of the 1st step - the 4th step of circuits 3-6 arrives at the output circuit 8 simultaneously through each latch circuitry 7. That is, each latch circuitry 7 is formed in order to take the synchronization of the digital output of each circuits 3-6.

[0134]The output circuit 8 carries out the after [a digital compensation process] parallel output of the 10-bit digital output Dout of the analog input signal Vin, when required.

[0135]As mentioned above, in the analog-to-digital circuit 1 of drawing 3. Although the voltage range of each part of the circuits 4-6 after the 2nd step became half [of the analog-to-digital circuit 100 of drawing 20] by using sub A/D converter 9b which has twice as many accuracy as this, the digital output same before a voltage range becomes half is obtained.

[0136]In this case, the alternating current component of current which flows through the circuits 3-6 of each stage decreases by optimizing a voltage range to sub A/D converter 9b which has twice as many accuracy as this, and setting it as a half. Thereby, the consumed electric current can provide the analog-to-digital circuit by which reduction was carried out by optimizing a voltage range, without changing a circuit design.

[0137](3) Circuitry drawing 4 of each part is a circuit diagram showing the 1st example of the composition of the arithmetic amplifier 11a in the analog-to-digital circuit 1 of drawing 1.

[0138]The arithmetic amplifier 11a of drawing 4 includes the operational amplifier 110, the capacity value switching circuit 111,112, the capacitor 113,114, and the switches 115-122. The switches 115-122 are constituted by the MOS (metal oxide semiconductor) transistor, for example.

[0139]The capacity value switching circuit 111 is connected as feed back capacity between the inversed input terminal of the operational amplifier 110, and an inverted output terminal, and the capacity value switching circuit 112 is connected as feed back capacity between the non-inversed input terminal and the noninverting output terminal. The capacitor 113 is connected to the inversed input terminal of the operational amplifier 110 as input capacitance, and the capacitor 114 is connected to the non-inversed input terminal as input capacitance.

[0140]The right side analog input voltage Vin (+) and middle reference voltage VRT1 are given to the capacitor 113 via the switch 115,116, respectively. The negative side analog input voltage Vin (-) and middle reference voltage VRT1 are given to the capacitor 114 via the switch 117,118, respectively. The inversed input terminal, the inverted output terminal, non-inversed input terminal, and noninverting output terminal of the operational amplifier 110 are grounded via the switch 119,120,121,122, respectively.

[0141]If capacity value of the capacitor 113,114 is set to CA, respectively and capacity value of the capacity value switching circuit 111,112 is set to CB here, respectively, The right side analog output voltage Vo of the inverted output terminal of the operational amplifier 110 (+) and the negative side analog output voltage Vo of a noninverting output terminal (-) become like a following formula.

[0142]

Vo(+) = (Vin(+)-VRT1) and (CA/CB)

Vo(-) = (Vin(-)-VRT1) and (CA/CB)

deltaVo=Vo(+)-Vo (-)

= (Vin(+)-Vin (-)) -(CA/CB)

Therefore, the profit of the arithmetic amplifier 11a can be changed by changing the capacity value CB of the capacity value switching circuit 111,112.

[0143]Drawing 5 is a circuit diagram showing the 2nd example of the composition of the arithmetic amplifier 11a in the analog-to-digital circuit 1 of drawing 1.

[0144]The arithmetic amplifier 11a of drawing 5 includes the operational amplifier 110, the capacitor 123,124, the capacity value switching circuit 125,126, and the switches 115-122.

[0145]The capacitor 123 is connected as feed back capacity between the inversed input terminal of the operational amplifier 110, and an inverted output terminal, and the capacitor 124 is

connected as feed back capacity between the non-inversed input terminal and the noninverting output terminal. The capacity value switching circuit 125 is connected to the inversed input terminal of the operational amplifier 110 as input capacitance, and the capacity value switching circuit 126 is connected to the non-inversed input terminal as input capacitance.
[0146]The right side analog input voltage Vin (+) and middle reference voltage VRT1 are given to the capacity value switching circuit 125 via the switch 115,116, respectively. The negative side analog input voltage Vin (-) and middle reference voltage VRT1 are given to the capacity value switching circuit 126 via the switch 117,118, respectively. The inversed input terminal, the inverted output terminal, non-inversed input terminal, and noninverting output terminal of the operational amplifier 110 are grounded via the switch 119,120,121,122, respectively.
[0147]If capacity value of the capacity value switching circuit 125,126 is set to CC, respectively and capacity value of the capacitor 123,124 is set to CD here, respectively, The right side analog output voltage Vo of the inverted output terminal of the operational amplifier 110 (+) and the negative side analog output voltage Vo of a noninverting output terminal (-) become like a following formula.
[0148]
Vo(+) = (Vin(+)-VRT1) and (CC/CD)
Vo(-) = (Vin(-)-VRT1) and (CC/CD)
deltaVo=Vo(+)-Vo (-)
= (Vin(+)-Vin (-)) -(CC/CD)
Therefore, the profit of the arithmetic amplifier 11a can be changed by changing capacity value CC of the capacity value switching circuit 125,126.
[0149]Drawing 6 - drawing 11 are the circuit diagrams showing the 1st - the 6th example of the concrete circuitry of the arithmetic amplifier 11a.
[0150]In drawing 6 - drawing 11, each of the capacitors Ca, Cb, and Cc shall have the equal capacity value C. Let m be arbitrary positive integers.
[0151]In the example of drawing 6, the parallel circuit and the switch Sa of m capacitor Ca are connected in series between the inversed input terminal of the operational amplifier 110, and an inverted output terminal, and the parallel circuit of m capacitor Ca is connected. Here, m is arbitrary positive integers. Similarly, the parallel circuit and the switch Sa of m capacitor Ca are connected in series between the non-inversed input terminal of the operational amplifier 110, and a noninverting output terminal, and the parallel circuit of m capacitor Ca is connected. The 2m piece capacitor Cb is connected to the inversed input terminal of the operational amplifier 110, and the 2m piece capacitor Cb is connected to the non-inversed input terminal.
[0152]The right side analog input voltage Vin (+) is given to the 2m piece capacitor Cb by the side of an inversed input terminal via the switch S1, respectively. The negative side analog input voltage Vin (-) is given to the capacitor Cb by the side of a non-inversed input terminal via the switch S1, respectively. The high potential side reference voltage VRT is given to the m capacitors Cb by the side of an inversed input terminal, and the m capacitors Cb by the side of a non-inversed input terminal via the switch S2, respectively, The low voltage side reference voltage VRB is given to the m capacitors Cb by the side of a non-inversed input terminal, and the m capacitors Cb by the side of a non-inversed input terminal via the switch S2, respectively.

[0153]In this example, the values of input capacitance are 2mC. If the switch Sa is carried out to one, the value of feed back capacity will serve as 2mC, and if the switch Sa is turned OFF, the value of feed back capacity will serve as mC. Therefore, at the time of a differential double end input, by changing the switch Sa to one, a profit will be 1 time and a profit will be twice by changing the switch Sa to OFF at the time of a single-ended input.
[0154]In the example of drawing 7, the parallel circuit of 2m piece capacitor Ca and the parallel circuit of 2m piece capacitor Cc are connected in series between the inversed input terminal of the operational amplifier 110, and an inverted output terminal, and the switch Sa is connected in parallel with capacitor Cc. Similarly, the parallel circuit of 2m piece capacitor Ca and the parallel circuit of 2m piece capacitor Cc are connected in series between the non-inversed input terminal of the operational amplifier 110, and a noninverting output terminal, and the switch Sa is

connected in parallel with capacitor Cc. The composition of other portions of the arithmetic amplifier 11a of drawing 7 is the same as that of the arithmetic amplifier 11a of drawing 6.
[0155]In this example, the values of input capacitance are 2mC. If the switch Sa is carried out to one, the value of feed back capacity will serve as 2mC, and if the switch Sa is turned OFF, the value of feed back capacity will serve as mC. Therefore, at the time of a differential double end input, by changing the switch Sa to one, a profit will be 1 time and a profit will be twice by changing the switch Sa to OFF at the time of a single-ended input.
[0156]In the example of drawing 8, the parallel circuit of 2m piece capacitor Ca and the parallel circuit of 2m piece capacitor Cc are connected in series between the inversed input terminal of the operational amplifier 110, and an inverted output terminal, and the switch Sa is connected in parallel with capacitor Ca. Similarly, the parallel circuit of 2m piece capacitor Ca and the parallel circuit of 2m piece capacitor Cc are connected in series between the non-inversed input terminal of the operational amplifier 110, and a noninverting output terminal, and the switch Sa is connected in parallel with capacitor Ca. The composition of other portions of the arithmetic amplifier 11a of drawing 8 is the same as that of the arithmetic amplifier 11a of drawing 6.
[0157]In this example, the values of input capacitance are 2mC. If the switch Sa is carried out to one, the value of feed back capacity will serve as 2mC, and if the switch Sa is turned OFF, the value of feed back capacity will serve as mC. Therefore, at the time of a differential double end input, by changing the switch Sa to one, a profit will be 1 time and a profit will be twice by changing the switch Sa to OFF at the time of a single-ended input.
[0158]In the example of drawing 9, the parallel circuit of m capacitor Ca is connected between the inversed input terminal of the operational amplifier 110, and the inverted output terminal. Similarly, the parallel circuit of m capacitor Ca is connected between the non-inversed input terminal of the operational amplifier 110, and the noninverting output terminal. The 2m piece capacitor Cb is connected to the inversed input terminal of the operational amplifier 110, and the 2m piece capacitor Cb is connected to the non-inversed input terminal.
[0159]The right side analog input voltage Vin (+) is given to the 2m piece capacitor Cb by the side of an inversed input terminal via the switch S1 and S1a, respectively. The negative side analog input voltage Vin (-) is given to the capacitor Cb by the side of a non-inversed input terminal via the switch S1 and S1a, respectively. The high potential side reference voltage VRT is given to the m capacitors Cb by the side of an inversed input terminal, and the m capacitors Cb by the side of a non-inversed input terminal via the switch S2 and S2a, respectively, The low voltage side reference voltage VRB is given to the m capacitors Cb by the side of a non-inversed input terminal, and the m capacitors Cb by the side of a non-inversed input terminal via the switch S2 and S2a, respectively.
[0160]In this example, the value of feed back capacity is mC. If the switch S1a and S2a are made one, the value of input capacitance will serve as 2mC, and if the switch S1a and S2a are turned OFF, the value of input capacitance will serve as mC. Therefore, at the time of a differential double end input, by always turning OFF the switch S1a and S2a, a profit will be 1 time and a profit will be twice by carrying out switching operation of the switch S1a and the S2a like the switch S1 and S2 at the time of a single-ended input.
[0161]In the example of drawing 10, the parallel circuit of m capacitor Ca is connected between the inversed input terminal of the operational amplifier 110, and the inverted output terminal. Similarly, the parallel circuit of m capacitor Ca is connected between the non-inversed input terminal of the operational amplifier 110, and the noninverting output terminal. The parallel circuit of 2m piece capacitor Cc is connected to the inversed input terminal of the operational amplifier 110, the 2m piece capacitor Cb is connected to the parallel circuit of capacitor Cc, and the switch Sa is connected in parallel with capacitor Cc. The parallel circuit of 2m piece capacitor Cc is connected to a non-inversed input terminal, the 2m piece capacitor Cb is connected to the parallel circuit of capacitor Cc, and the switch Sa is connected in parallel with capacitor Cc. The composition of other portions of the arithmetic amplifier 11a of drawing 10 is the same as that of the arithmetic amplifier 11a of drawing 6.
[0162]In this example, the value of feed back capacity is mC. If the switch Sa is carried out to one, the value of input capacitance will serve as 2mC, and if the switch Sa is turned OFF, the

value of input capacitance will serve as mC. Therefore, at the time of a differential double end input, by turning OFF the switch Sa, a profit will be 1 time and a profit will be twice by carrying out the switch Sa to one at the time of a single-ended input.

[0163]In the example of drawing 11, the parallel circuit of m capacitor Ca is connected between the inversed input terminal of the operational amplifier 110, and the inverted output terminal. Similarly, the parallel circuit of m capacitor Ca is connected between the non-inversed input terminal of the operational amplifier 110, and the noninverting output terminal. The parallel circuit of 2m piece capacitor Cc is connected to the inversed input terminal of the operational amplifier 110, the 2m piece capacitor Cb is connected to the parallel circuit of capacitor Cc, and the switch Sa is connected to the capacitor Cb in parallel. The parallel circuit of 2m piece capacitor Cc is connected to a non-inversed input terminal, the 2m piece capacitor Cb is connected to the parallel circuit of capacitor Cc, and the switch Sa is connected to the capacitor Cb in parallel. The composition of other portions of the arithmetic amplifier 11a of drawing 11 is the same as the composition of the arithmetic amplifier 11a of drawing 6.

[0164]In this example, the value of feed back capacity is mC. If the switch Sa is carried out to one, the value of input capacitance will serve as 2mC, and if the switch Sa is turned OFF, the value of input capacitance will serve as mC. Therefore, at the time of a differential double end input, by turning OFF the switch Sa, a profit will be 1 time and a profit will be twice by carrying out the switch Sa to one at the time of a single-ended input.

[0165]In the arithmetic amplifier 11a of drawing 6 - drawing 11, the switch Sa is constituted by the MOS transistor as mentioned above. The diffusion capacitance of a MOS transistor is added to the node to which the switch Sa is connected by that cause, and gate capacitance is added at the time of one of the switch Sa. If capacity is added to the inversed input terminal or non-inversed input terminal of the operational amplifier 110, the working speed of the arithmetic amplifier 11a will fall.

[0166]The switch Sa is connected to the inverted output terminal and noninverting output terminal of the operational amplifier 110 in the example of drawing 6 and drawing 7. Thereby, the working speed of the arithmetic amplifier 11a does not fall. Therefore, the example of drawing 6 and drawing 7 is preferred.

[0167]Since on resistance exists at the time of one of the switch Sa when the switch Sa is connected in parallel with a capacitor, the capacity of a capacitor is thoroughly unseparable.

[0168]In the example of drawing 6, the switch Sa is connected to capacitor Ca in series, and the switch Sa is connected to the inverted output terminal and noninverting output terminal of the operational amplifier 110. Thereby, the capacity of capacitor Ca is thoroughly separable at the time of one of the switch Sa. Therefore, the example of drawing 6 is the most preferred.

[0169]In the example of drawing 9, the switch S1a and S2a are connected to the input side rather than the capacitor Cb. On the contrary, when the capacitor Cb is connected to the input side rather than the switch S1a and S2a, even if the switch S1a and S2a are set as an OFF state, the parasitic capacitance of the capacitor Cb is charged. By that cause, it will be necessary to take parasitic capacitance into consideration, and a profit will vary with dispersion in parasitic capacitance at the time of setting out of a profit. Like the example of drawing 9, by connecting the switch S1a and S2a to an input side rather than the capacitor Cb, when the switch S1a and S2a are set as an OFF state, the capacitor Cb is separated by the switch S1a and S2a with parasitic capacitance. Therefore, in the example of drawing 9, it becomes unnecessary to take the parasitic capacitance of the capacitor Cb into consideration at the time of setting out of a profit, and dispersion in the profit by dispersion in parasitic capacitance is lost.

[0170]The circuit diagram showing the 1st example of the composition of sub A/D converter [in / in drawing 12 / the analog-to-digital circuit 1 of drawing 1] 9a and drawing 13 are the circuit diagrams showing the composition of the comparator used for sub A/D converter 9a of drawing 12.

[0171]Sub A/D converter 9a is provided with the circuit generating reference voltage 92, 93a, and 93b and two or more comparators 90 which generate reference voltage in drawing 12.

[0172]The circuit generating reference voltage 92 consists of two or more resistance R

connected in series. The circuit generating reference voltage 93a consists of two or more resistance R connected in series. The circuit generating reference voltage 93b consists of two or more resistance R1 connected in series. Two or more resistance R has equal resistance, and two or more resistance R1 has equal resistance.

[0173]The circuit generating reference voltage 92 is connected between the node N91 which receives the high potential side reference voltage VRT, and the node N92 which receives the low voltage side reference voltage VRB. The circuit generating reference voltage 93a is connected via the switch S24 and S25 between the node N93 which receives the high potential side reference voltage VRT, and the node N94 which receives the low voltage side reference voltage VRB. The circuit generating reference voltage 93b is connected between the node N93 which receives the high potential side reference voltage VRT, and the node N94 which receives the low voltage side reference voltage VRB. The switch S26 is connected between the intermediate node N95 of the circuit generating reference voltage 93a, and the intermediate node N96 of the circuit generating reference voltage 93b.

[0174]Reference voltage which is different at the node during the resistance R of the circuit generating reference voltage 92, respectively is generated. Similarly, reference voltage which is different at the node during the resistance R of the circuit generating reference voltage 93a, respectively is generated. Here, different reference voltage obtained by the circuit generating reference voltage 92 is called the right side reference voltage Vref (+). Different reference voltage obtained by the circuit generating reference voltage 93a is called the negative side reference voltage Vref (−).

[0175]Middle reference voltage VRT1 (=(VRT−VRB)/2) which is the middle voltage of the high potential side reference voltage VRT and the low voltage side reference voltage VRB is generated by the intermediate node N96 of the circuit generating reference voltage 93b.

[0176]As shown in drawing 13, each comparator 90 includes the operational amplifier 91, the capacitor C1, C2, and the switches S13−S18. The switch S13 is connected between the inversed input terminal of the operational amplifier 91, and an inverted output terminal, and the switch S14 is connected between the non−inversed input terminal and the noninverting output terminal. The capacitor C1 is connected to the inversed input terminal of the operational amplifier 91, and the capacitor C2 is connected to the non−inversed input terminal. The switch S15 and S16 are connected to the capacitor C1, and the switch S17 and S18 are connected to the capacitor C2. In drawing 12, the switch S13 of each comparator 90 and the graphic display of S14 are omitted.

[0177]The right side analog input voltage Vin (+) and the right side reference voltage Vref (+) are given to the capacitor C1 via the switch S15 and S16, respectively. The negative side analog input voltage Vin (−) and the negative side reference voltage Vref (−) are given to the capacitor C2 via the switch S17 and S18, respectively.

[0178]In the initial state, and the switch S16 and S18 turn off. [the switch S13 S14, S15, and S17] Next, the one [the switch S15 and S17 are turned off and / the switch S16 and S18] after turning off the switch S13 and S14. Since the inversed input terminal and non−inversed input terminal of the operational amplifier 91 are floating when the switch S13 and S14 are turned off, The voltage of an inversed input terminal changes (Vin(+)−Vref (+)), and the voltage of a non−inversed input terminal changes (Vin(−)−Vref (−)). As a result, differential analog input voltage (Vin(+)−Vin (−)) and differential reference voltage (Vref(+)−Vref (−)) are measured, and right side analog−output−voltage Vout (+) and negative side analog−output−voltage Vout (−) change according to a comparison result.

[0179]The digital code Dcode can be obtained by encoding the comparison result of two or more comparators 90 of drawing 12 with the encoder 950.

[0180]In sub A/D converter 9a of drawing 12, at the time of a differential double end input, and the switch S26 is turned off. [the switch S24 and S25] Thereby, the negative side reference voltage Vref (−) which changes with circuit generating reference voltage 93a via the switch S18, respectively to the capacitor C2 of each comparator 90 is given. At the time of a single−ended input, the switch S24 and S25 are turned off and the switch S26 is carried out to one. Thereby, middle reference voltage VRT1 is given to the capacitor C2 of each comparator 90 by the circuit generating reference voltage 93b via the switch S18.

[0181]Thus, a full-scale range is changed in sub A/D converter 9a.
[0182]The switch S26 may be connected between the intermediate node N95 of the circuit generating reference voltage 93a, and the intermediate node of the circuit generating reference voltage 92, without forming the circuit generating reference voltage 93b.
[0183]The circuit diagram showing the 2nd example of the composition of sub A/D converter [in / in drawing 14 / the analog-to-digital circuit 1 of drawing 1] 9a and drawing 15 are the circuit diagrams showing the composition of the comparator used for sub A/D converter 9a of drawing 14.
[0184]In drawing 14, the switch S26 of drawing 12 is not connected between the intermediate node N95 of the circuit generating reference voltage 93a, and the intermediate node N96 of the circuit generating reference voltage 93b.
[0185]As shown in drawing 15, each comparator 90 includes the operational amplifier 91, the capacitor C1, C2, and the switches S13-S18, and contains the switch S21 and S22 further. One end of the switch S21 is connected to the capacitor C1, and the other end of the switch S21 is opened wide. One end of the switch S22 is connected to the capacitor C2, and the other end is connected to the intermediate node N96 of the reference voltage generating time 93b of drawing 14. The composition of other portions of the comparator 90 of drawing 15 is the same as the composition of the comparator 90 of drawing 13.
[0186]Middle reference voltage VRT1 is given to the capacitor C2 by the reference voltage generating time 93b via the switch S22.
[0187]Operation of the comparator 90 of drawing 15 at the time of a differential double end input is the same as operation of the comparator 90 of drawing 13. At this time, the switch S21 and S22 are always turned off. At the time of a single-ended input, the switch S22 is operated instead of the switch S18. At this time, the switch S21 is always turned off.
[0188]The one [the switch S24 and S25] at the time of a differential double end input in sub A/D converter 9a of drawing 14. At this time, the switch S21 and S22 are always turned OFF. Thereby, the negative side reference voltage Vref (-) which changes with circuit generating reference voltage 93a via the switch S18, respectively to the capacitor C2 of each comparator 90 is given. At the time of a single-ended input, the switch S24 and S25 are turned off and the switch S22 is operated instead of the switch S18. At this time, the switch S21 is always turned off. Thereby, middle reference voltage VRT1 is given to the capacitor C2 of each comparator 90 by the circuit generating reference voltage 93b via the switch S22.
[0189]Thus, a full-scale range is changed in sub A/D converter 9a.
[0190]Although it is not necessary to form the switch S21 in each comparator 90, in order to secure the symmetry of the circuitry of the comparator 90, it is preferred to form the switch S21.
[0191]Drawing 16 is a circuit diagram of sub A/D converter 9b in the 2nd step of circuit 4 in the analog-to-digital circuit 1 of drawing 3. Sub A/D converter 9b of drawing 16 is a full-parallel comparison (flash plate) method sub A/D converter.
[0192]Sub A/D converter 9b comprises the circuit generating reference voltage 94 and 95 and two or more comparators 90 which generate reference voltage. Each of the circuit generating reference voltage 94 and 95 consists of the resistance R2 or 2n resistance R of a piece and, and the resistance R3. The resistance R2 and R3 have resistance n times the resistance of R, respectively. The resistance R2 or 2n resistance R of a piece and, and the resistance R3 are connected between the node N97 which receives high potential side reference voltage VRT2, and the node N98 which receives low voltage side reference voltage VRB2. The switch S28 is connected to the both ends of the resistance R2, and the switch S29 is connected to the both ends of the resistance R3.
[0193]Reference voltage which is different at the node during the resistance R of the circuit generating reference voltage 94, respectively is generated. Similarly, reference voltage which is different at the node during the resistance R of the circuit generating reference voltage 95, respectively is generated. Here, different reference voltage obtained by the circuit generating reference voltage 94 is called the right side reference voltage Vref (+). Different reference voltage obtained by the circuit generating reference voltage 95 is called the negative side

reference voltage Vref (−).
[0194]The right side analog input voltage Vin (+) and the right side reference voltage Vref (+) are given to the capacitor C1 of each comparator 90 via the switch S15 and S16, respectively. The negative side analog input voltage Vin (−) and the negative side reference voltage Vref (−) are given to the capacitor C2 of each comparator 90 via the switch S17 and S18, respectively. The composition and operation of the comparator 90 of drawing 16 are the same as the composition of the comparator 90 of drawing 13, and operation.
[0195]Here, the difference of high potential side reference voltage VRT2 and low voltage side reference voltage VRB2 is set as $VIN_{p-p}/8$. When the switch S28 of the circuit generating reference voltage 95 and 96 and S29 are OFF, full-scale ranges are $VIN_{p-p}/16$. If the switch S28 and S29 are made one, a full-scale range will be set to $VIN_{p-p}/8$. Thus, in sub A/D converter 9b, a full-scale range can be changed 1 time and twice.
[0196]Drawing 17 is a circuit diagram of D/A converter 10 in the 2nd step of circuit 4 in the analog-to-digital circuit 1 of drawing 3. D/A converter 10 of drawing 17 is a capacity array method D/A converter.
[0197]D/A converter 10 comprises the switch S51 by the side of right [of the each plurality connected to the circuit generating reference voltage 96 which generates reference voltage, and array form], S52 and the switch S53 of two or more negative sides, S54, two or more right side capacitors C50, and two or more negative side capacitors C51.
[0198]The circuit generating reference voltage 96 consists of the resistance R4, two or more resistance R, and the resistance R5. The resistance R4 and R5 have the resistance of the half of the resistance of the sum total of two or more resistance R. The resistance R4, two or more resistance R, and the resistance R5 are connected in series between the node N101 which receives high potential side reference voltage VRT3, and the node N102 which receives low voltage side reference voltage VRB3. The switch S30 is connected to the both ends of the resistance R4, and the switch S31 is connected to the both ends of the resistance R5.
[0199]All of the capacitor C50 and C51 have the same capacity value. From one terminal (it is hereafter called an output terminal) N111 of the capacitor C50, the differential positive side output voltage VDA (+) is generated, and the differential negative side output voltage VDA (−) is generated from one terminal (henceforth an output terminal) N112 of the capacitor C51. Each capacitor C50 and the terminal of another side of C51 are called an input terminal.
[0200]One terminal of each switch S51 is connected to the node N103 between the resistance R4 and the resistance R, and the terminal of another side is connected to the input terminal of the capacitor C50. One terminal of each switch S52 is connected to the node N104 between the resistance R5 and the resistance R, and the terminal of another side is connected to the input terminal of the capacitor C50. One terminal of each switch S53 is connected to the node N103 between the resistance R4 and the resistance R, and the terminal of another side is connected to the input terminal of the capacitor C51. One terminal of each switch S54 is connected to the node N104 between the resistance R5 and the resistance R, and the terminal of another side is connected to the input terminal of the capacitor C51.
[0201]According to the output level of the comparator 90 of sub A/D converter 9b of drawing 16, on-off control action of the switch S51, S52, S53, and S54 is carried out. The four switches S51 which receive the output signal of the same comparator 90, S52, S53, and S54 constitute 4 ream switch. For example, when the output of the one comparator 90 is high-level, and the switch S52 and S53 turn off. [the switch S51 of 4 ream switch, and S54] On the contrary, one [the switch S51 of 4 ream switch and S54 turn off, and / the switch S52 and S53] when the output of the one comparator 90 is a low level.
[0202]According to the output level of two or more comparators 90 of sub A/D converter 9b, two or more switches S51, S52, S53, and S54 carry out on-off control action, and the differential positive side output voltage VDA (+) and the differential negative side output voltage VDA (−) are obtained by the output terminal N111 and N112.
[0203]Here, the difference of high potential side reference voltage VRT3 and low voltage side

reference voltage VRB3 is set as $VIN_{p-p}/4$. When the switch S30 of the circuit generating reference voltage 96 and S31 are OFF, full-scale ranges are $VIN_{p-p}/8$. If the switch S30 and S31 are made one, a full-scale range will be set to $VIN_{p-p}/4$. Thus, in D/A converter 10b, a full-scale range can be changed 1 time and twice.

[0204]Drawing 18 is a circuit diagram showing the 1st example of the composition of the subtraction amplifier 14a in the analog-to-digital circuit 1 of drawing 3.

[0205]The subtraction amplifier 14a of drawing 18 includes the operational amplifier 130, the capacity value switching circuit 131,132, the capacitor 133,134, and the switches 135-138. A switch is constituted by the MOS (metal oxide semiconductor) transistor, for example.

[0206]The capacity value switching circuit 131 is connected as feed back capacity between the inversed input terminal of the operational amplifier 130, and an inverted output terminal, and the capacity value switching circuit 132 is connected as feed back capacity between the non-inversed input terminal and the noninverting output terminal. The capacitor 133 is connected to the inversed input terminal of the operational amplifier 130 as input capacitance, and the capacitor 134 is connected to the non-inversed input terminal as input capacitance.

[0207]The differential positive side output voltage VDA (+) outputted from the right side analog output voltage Vo (+) and D/A converter 10b which are outputted is given to the capacitor 133 via the switch 135,136, respectively from the arithmetic amplifier 11 of drawing 3. The differential positive side output voltage VDA (-) outputted from the negative side analog output voltage Vo (-) and D/A converter 10b which are outputted is given to the capacitor 134 via the switch 137,138, respectively from the arithmetic amplifier 11. The inversed input terminal, the inverted output terminal, non-inversed input terminal, and noninverting output terminal of the operational amplifier 130 are grounded via the switch 139,140,141,142, respectively.

[0208]Operation of the subtraction amplifier 14a of drawing 18 is the same as operation of the arithmetic amplifier 11a of drawing 4. The right side analog input voltage Vin (+) and the negative side analog input voltage Vin (-) which are given in the circuit 4 of the next step are obtained from the inverted output terminal and noninverting output terminal of the operational amplifier 130.

[0209]Here, the profit of the subtraction amplifier 14a can be changed by changing the capacity value of the capacity value switching circuit 131,132.

[0210]Drawing 19 is a circuit diagram showing the 2nd example of the composition of the subtraction amplifier 14a in the analog-to-digital circuit 1 of drawing 3.

[0211]The subtraction amplifier 14a of drawing 19 includes the operational amplifier 130, the capacitor 139,140, the capacity value switching circuit 141,142, and the switches 135-140.

[0212]The capacitor 139 is connected as feed back capacity between the inversed input terminal of the operational amplifier 130, and an inverted output terminal, and the capacitor 140 is connected as feed back capacity between the non-inversed input terminal and the noninverting output terminal. The capacity value switching circuit 141 is connected to the inversed input terminal of the operational amplifier 130 as input capacitance, and the capacity value switching circuit 142 is connected to the non-inversed input terminal as input capacitance.

[0213]The differential positive side output voltage VDA (+) outputted from the right side analog output voltage Vo (+) and D/A converter 10b which are outputted is given to the capacity value switching circuit 141 via the switch 135,136, respectively from the arithmetic amplifier 11 of drawing 3. The differential positive side output voltage VDA (-) outputted from the negative side analog output voltage Vo (-) and D/A converter 10b which are outputted is given to the capacity value switching circuit 142 via the switch 137,138, respectively from the arithmetic amplifier 11. The inversed input terminal, the inverted output terminal, non-inversed input terminal, and noninverting output terminal of the operational amplifier 130 are grounded via the switch 139,140,141,142, respectively.

[0214]Operation of the subtraction amplifier 14a of drawing 19 is the same as operation of the arithmetic amplifier 11a of drawing 5. The right side analog input voltage Vin (+) and the negative side analog input voltage Vin (-) which are given in the circuit 4 of the next step are obtained from the inverted output terminal and noninverting output terminal of the operational amplifier

130.
[0215]Here, the profit of the subtraction amplifier 14a can be changed by changing the capacity value of the capacity value switching circuit 141,142.
[0216]The switch Sa of the above-mentioned embodiment, S1a, S2a, S24, S25, S26, S28, S29, S30, and S31 are formed, for example of an MOS (metal oxide semiconductor) field effect transistor.
[0217]According to the above-mentioned embodiment, the switch Sa, S1a, S2a, S24, S25, S26, S28, S29, S30, and S31 are used as a switch part of a switching means. In this case, the switch Sa, S1a, S2a, S24, S25, S26, S28, S29, S30, and S31 can be changed to one or OFF at the time of manufacture or use. The switch part of a switching means is not limited to a switch. For example, the fuse which can be blown out with laser may be used as a switch part, and the mask switch part for patterning of top layer metal may be used as a switch part.
[0218]Drawing 20 is a circuit diagram showing other examples of a switch part. In the example of drawing 20, the fuse Fa is used instead of the switch Sa of the arithmetic amplifier 11a of drawing 6. The fuse Fa can consist of polysilicon, for example, and can be blown out with laser. At the time of manufacture, the profit of the arithmetic amplifier 11a can be changed by whether laser is used and the fuse Fa is blown out.
[0219]Drawing 21 and drawing 22 are the figures showing the example of further others of a switch part, show a top view to the upper part and show a sectional view to the lower part.
[0220]In the capacity formation section C500, the electrode 501,502 of the capacitor is formed of lower layer metal LM1 and LM2. The electrode 507,508 is formed of lower layer metal LM1. With the top layer metal UM, the electrode 512,513 is formed with a prescribed interval, and the electrode 514,515 is formed with the prescribed interval. The electrode 501 is connected to the electrode 512 via the metal in the through hole 503, and the electrode 502 is connected to the electrode 514 via the metal in the through hole 504. The electrode 507 is connected to the electrode 512 via the metal in the through hole 505, and the electrode 508 is connected to the electrode 515 via the metal in the through hole 506.
[0221]For example, 507 is connected to the inversed input terminal of the operational amplifier 110 of drawing 6, and the electrode 508 is connected to the inverted output terminal of the operational amplifier 110 of drawing 6.
[0222]The capacity formation section C500 is formed of the electrode 501,502, and mask switch part municipal solid waste is formed between the electrodes 512,513 and of between the electrodes 514,515, respectively. The capacity formation block C500 is equivalent to capacitor Ca of drawing 6, for example.
[0223]At the time of manufacture, between the electrodes 512,513 and between the electrodes 514,515 can be changed to a connected state and a cut off state by changing the pattern of the mask arranged on mask switch part municipal solid waste.
[0224]As shown in drawing 21, between the electrodes 512,513 and between the electrodes 514,515 are connectable by using the mask that the metal layer 510,511 is formed with the top layer metal UM between the electrodes 512,513 and between the electrodes 514,515.
[0225]As shown in drawing 22, between the electrodes 512,513 and between the electrodes 514,515 can be intercepted by using the mask that a metal layer is not formed with the top layer metal UM between the electrodes 512,513 and between the electrodes 514,515.
[0226]In the example of drawing 21 and drawing 22, the capacity formation section C500 is thoroughly separable from an operational amplifier by providing a mask switch part in the terminal of both capacity formation sections C500, respectively.
[0227]In the circuit of the stages with an arbitrary analog-to-digital circuit in which this invention is not limited to the above-mentioned embodiment, At least one of the D/A converters which have an arithmetic amplifier which has a switchable profit, a subtraction amplifier which has a switchable profit, a sub A/D converter which has a switchable full-scale range, and a switchable full-scale range may be used.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]Here, when the voltage range of the analog input signal Vin is made into VIN_{p-p}, the full-scale range of sub A/D converter 9 in the 1st step of circuit 3 is equal to voltage range VIN_{p-p} of an analog input signal in the above-mentioned analog-to-digital circuit 100. The full-scale range of sub A/D converter 9 in the 2-4th step of circuit 4-6 is equal to output voltage range $VIN_{p-p}/8$ of the subtraction amplifier 14 of the 1-3rd step of circuits 3-5 respectively.
[0009]The full-scale range of D/A converter 10 in the 1st step of circuit 3 is equal to voltage range VIN_{p-p} of the analog input signal Vin like sub A/D converter 9. The full-scale range of the voltage of D/A converter 10 in the 2nd step and the 3rd step of circuit 4 and 5 is set to VIN[as the full-scale range of sub A/D converter 9] $_{p-p}$ twice many / 4 in order to take consistency with the output voltage range of the arithmetic amplifier 11 which has the profit 2.
[0010]Next, operation of the analog-to-digital circuit 1 of drawing 23 is explained. The sample hold circuit 2 samples the analog input signal Vin, and carries out fixed time maintenance. The analog input signal Vin outputted from the sample hold circuit 2 is transmitted to the 1st step of circuit 3.
[0011]In the 1st step of circuit 3, sub A/D converter 9 performs an analog to digital to the analog input signal Vin of voltage range VIN_{p-p}. Here, the full-scale range of sub A/D converter 9 is VIN_{p-p} as mentioned above. The digital output (2^9, 2^8, 2^7, 2^6) which is an analog-to-digital result of sub A/D converter 9 is transmitted to the output circuit 8 via the four latch circuitry 7 while it is transmitted to D/A converter 10. The normal output voltage range of D/A converter 10 is expressed like a following formula.
[0012]
(The 1st step of resolution-1) x(full-scale range of D/A converter 10)/(the 1st step of resolution)
$= (2^4-1) \times (VIN_{p-p}) / 2^4 = 15VIN_{p-p}/16$ one side and the arithmetic amplifier 11 sample the analog input signal Vin, and amplify and hold it. The output voltage range of the arithmetic amplifier 11 is expressed like a following formula.
[0013]
(Voltage range VIN_{p-p} of the analog input signal Vin) x (profit of the arithmetic amplifier 11)
= The $VIN_{p-p} \times 1 = VIN_{p-p}$ subtraction amplifier 14 subtracts and amplifies the analog input signal Vin and the D/A conversion result of D/A converter 10 which were outputted from the arithmetic amplifier 11. The output of the subtraction amplification width circuit 14 is transmitted to the 2nd step of circuit 4. The output voltage range of the 1st step of subtraction amplifier 14 is expressed like a following formula.
[0014]
(Output voltage range of the arithmetic amplifier 11) x (- (normal output voltage range of D/A converter 10)) (profit of the subtraction amplifier 14)

= (VIN_{p-p}) (- (15VIN_{p-p}/16)) In the x2 =VIN_{p-p}/82 step circuit 4, sub A/D converter 9 performs an A/D conversion to the output of the subtraction amplifier 14 of the 1st step of circuit 3. The A/D conversion result of sub A/D converter 9 is transmitted to the output circuit 8 via the three latch circuitry 7 while it is transmitted to D/A converter 10.Thereby, a 2-bit digital output (2^5, 2^4) is obtained at least for Nakagami from the 2nd step of circuit 4. The normal output voltage range of D/A converter 10 is expressed like a following formula.

[0015]

(The 2nd step of resolution-1) x(full-scale range of D/A converter 10)/(the 2nd step of resolution)

= (2^2-1) x (VIN_{p-p}/4) / 2^2=3VIN_{p-p}/16 one side and the arithmetic amplifier 11 amplify the output of the arithmetic amplifier 13 of the 1st step of circuit 3. The output voltage range of the arithmetic amplifier 11 is expressed like a following formula.

[0016]

(Output voltage range of the 1st step of subtraction amplifier 14) x (profit of the arithmetic amplifier 11)

= (VIN_{p-p}/8) The x2 =VIN_{p-p}/4 subtraction amplifier 14 subtracts and amplifies the output of the arithmetic amplifier 11, and the D/A conversion result of D/A converter 10. The output of the subtraction amplifier 14 is transmitted to the 3rd step of circuit 5. The range of the output voltage of the 2nd step of subtraction amplifier 14 is expressed like a following formula.

[0017]

(Output voltage range of the arithmetic amplifier 11) x (- (normal output voltage range of D/A converter 10)) (profit of the subtraction amplifier 14)

= (VIN_{p-p}/4) (- (3VIN_{p-p}/16)) In the x2 =VIN_{p-p}/83 step circuit 5, the same operation as the 2nd step of circuit 4 is performed to the output of the subtraction amplifier 14 of the 2nd step of circuit 3. Thereby, a 2-bit digital output (2^3, 2^2) is obtained at least for Nakashita from the 3rd step of circuit 5. The output voltage range of each part is the same as that of the 2nd step of circuit 4.

[0018]In the 4th step of circuit 6, sub A/D converter 9 performs an A/D conversion to the output of the subtraction amplifier 14 of the 3rd step of circuit 5, and the digital output (2^1, 2^0) of 2 bits of low ranks is obtained.

[0019]The digital output of the 1st step - the 4th step of circuits 3-6 arrives at the output circuit 8 simultaneously through each latch circuitry 7. That is, each latch circuitry 7 is formed in order to take the synchronization of the digital output of each circuits 3-6.

[0020]The output circuit 8 carries out the after [a digital compensation process] parallel output of the 10-bit digital output Dout of the analog input signal Vin, when required.

[0021]Thus, even if the conversion number of bits increases and LSB (Least Significant Bit) becomes small with reduction in power supply voltage, the resolution of sub A/D converter 9 can be raised and sufficient conversion precision is acquired.

[0022]Drawing 24 (a) is a figure for the circuit diagram and drawing 24 (b) in which the composition of the subtraction amplifier of the analog-to-digital circuit of drawing 23 is shown to explain operation of the subtraction amplifier of drawing 24 (a).

[0023]In drawing 24, the inversed input terminal of the operational amplifier 101 is connected to the node nb, and the non-inversed input terminal is grounded. The output terminal of the operational amplifier 101 is connected to the inversed input terminal via the capacitor 102 while being connected to the node no. Switch SW1 is connected between the inversed input terminal of the operational amplifier 1, and a non-inversed input terminal, and the capacitor 103 is connected between the node nb and the node na. It is connected to the node n1 via switch SW2, and the node na is connected to the node n2 via switch SW3. These switch SW2 and SW3 are constituted by the CMOS switch which usually consists of a CMOS (complementary-type metal oxide semiconductor) field effect transistor.

[0024]Voltage V_1 is inputted into the node n1, voltage V_2 is inputted into the node n2, and

voltage V_O is outputted from the node no.

[0025]Here, operation of the subtraction amplifier of drawing 24 (a) is explained, referring to drawing 24 (b). Capacity value of the capacitor 101 is set to C, capacity value of the capacitor 103 is set to KC, and earth potentials are made into V_G. K is a constant.

[0026]First, switch SW1 and switch SW2 are made one, and switch SW3 is turned OFF. Thereby, the voltage of the node na serves as V_1. The voltage of the node no is set to 0. At this time, the electric charge Qa of the node nb becomes like a following formula.

[0027]After turning OFF $Qa=(V_G-V_1)$ KC, next switch SW1, switch SW2 is turned OFF and switch SW3 is made one. Thereby, the voltage of the node na serves as V_2. The voltage of the node no serves as V_O. In order to carry out the imaginary earth of the node nb at this time, the electric charge Qb of the node nb becomes like a following formula.

[0028]

Since there is no course out of which an electric charge escapes from and comes in the $Qb=(V_G-V_2)$ $KC+(V_G-V_O)$ C node nb, it becomes Qa=Qb with conservation of charge. Therefore, a following formula is materialized.

[0029](V_G-V_1) Voltage V_O of a $KC=(V_G-V_2)$ $KC+(V_G-V_O)$ C top type to the node no becomes like a following formula.

[0030]Voltage V_2 is subtracted from $V_O=V_G+(V_1-V_2)$ K, thus voltage V_1, and the subtraction value is amplified K times.

[0031]Therefore, a subtraction amplifier has a function which outputs the difference of voltage V_1 and voltage V_2 by the profit decided by the capacity factor of the capacitor 103 and the capacitor 102. For example, a sample hold function 1 time the profit of this will be given to a subtraction amplifier by setting it as KC=C (K= 1).

[0032]Drawing 25 is a figure showing the composition of the sub A/D converter used in the analog-to-digital circuit of drawing 23.

[0033]Two or more comparators 900 are arranged in the parallel connected type analog-digital converter 9 of drawing 25. The analog input voltage Vin is given to one input terminal of two or more comparators 900, and the reference voltage obtained by carrying out the partial pressure of the voltage between the high potential side reference voltage VRT and the low voltage side reference voltage VRB to the input terminal of another side by two or more resistance R is given, respectively. Each comparator 900 compares the voltage of one input terminal with the voltage of the input terminal of another side. The digital code Dcode can be obtained by encoding the comparison result of two or more comparators 900 with the encoder 910.

[0034]By the way, when the voltage range of the analog input signal given to an analog-to-digital circuit is changed, Or to change the method of the analog input signal given to an analog-to-digital circuit in a differential double end input and a single-ended input, it is necessary to change the specification of an analog-to-digital circuit.

[0035]Here, a differential double end input and a single-ended input are explained. Drawing 26 (a) and (b) is a figure for explaining the analog to digital in a differential double end input and a single-ended input. A horizontal axis shows the analog input voltage VIN, and a vertical axis shows the outputted digital code Dcode.

[0036]As shown in drawing 26 (a), at the time of a differential double end input, the right side analog input voltage Vin (+) and the negative side analog input voltage Vin (-) of the analog input signal Vin change complementarily. Thereby, the difference of the right side analog input voltage Vin (+) and the negative side analog input voltage Vin (-) serves as voltage range VIN_{p-p} of the analog input signal Vin.

[0037]Therefore, as shown in drawing 26 (a), the right side analog input voltage Vin (+) changes from 1.0V in 2.0, When the negative side analog input voltage Vin (-) changes in 2.0V to 1.0V, the voltage range of the analog input signal Vin is set to 2.0V from the operation of Vin(+)-Vin (-).

[0038]On the other hand, as shown in drawing 26 (b), at the time of a single-ended input, the

right side analog input voltage Vin (+) changes. Thereby, the voltage range of the right side analog input voltage Vin (+) turns into a voltage range of the analog input signal Vin.

[0039]Therefore, as shown in drawing 26 (b), when the right side analog input voltage Vin (+) changes in 1.0V to 2.0V, the voltage range of an analog input signal is set to 1.0V.

[0040]That is, if the voltage range of the analog input signal Vin of a differential double end input method is made into $2VIN_{p-p}$, the voltage range of the analog input signal Vin of a single-ended input method will serve as VIN_{p-p}.

[0041]Thus, with a differential double end input method and a single-ended input method, even if the range of change of each analog input voltage is the same, the voltage ranges of an analog input signal will differ.

[0042]In the above-mentioned conventional analog-to-digital circuit, when changing the voltage range of an analog input signal, or when changing the input method of an analog input signal, it is necessary to redesign circuitry.

[0043]The purpose of this invention is to provide the pipeline type analog-to-digital circuit which can change the input method between change of the voltage range of an analog input signal or a differential double end input, and a single-ended input easily without redesigning circuitry.

[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a block diagram showing the composition of the pipeline type analog-to-digital circuit in a 1st embodiment of this invention.
[Drawing 2]It is a figure showing setting out in the case of changing the analog-to-digital circuit of drawing 1 to a differential double end input method and a single-ended input method, respectively.
[Drawing 3]It is a block diagram showing the composition of the pipeline type analog-to-digital circuit in a 2nd embodiment of this invention.
[Drawing 4]It is a circuit diagram showing the 1st example of the composition of the arithmetic amplifier in the analog-to-digital circuit of drawing 1.
[Drawing 5]It is a circuit diagram showing the 2nd example of the composition of the arithmetic amplifier in the analog-to-digital circuit of drawing 1.
[Drawing 6]It is a circuit diagram showing the 1st example of the concrete circuitry of an arithmetic amplifier.
[Drawing 7]It is a circuit diagram showing the 2nd example of the concrete circuitry of an arithmetic amplifier.
[Drawing 8]It is a circuit diagram showing the 3rd example of the concrete circuitry of an arithmetic amplifier.
[Drawing 9]It is a circuit diagram showing the 4th example of the concrete circuitry of an arithmetic amplifier.
[Drawing 10]It is a circuit diagram showing the 5th example of the concrete circuitry of an arithmetic amplifier.
[Drawing 11]It is a circuit diagram showing the 6th example of the concrete circuitry of an arithmetic amplifier.
[Drawing 12]It is a circuit diagram showing the 1st example of the composition of the sub A/D converter in the analog-to-digital circuit of drawing 1.
[Drawing 13]It is a circuit diagram showing the composition of the comparator used for the sub A/D converter of drawing 12.
[Drawing 14]It is a circuit diagram showing the 2nd example of the composition of the sub A/D converter in the analog-to-digital circuit of drawing 1.
[Drawing 15]It is a circuit diagram showing the composition of the comparator used for the sub A/D converter of drawing 14.
[Drawing 16]It is a circuit diagram of the sub A/D converter in the 2nd step of circuit in the analog-to-digital circuit of drawing 3.
[Drawing 17]It is a circuit diagram of the D/A converter in the 2nd step of circuit in the analog-to-digital circuit of drawing 3.
[Drawing 18]It is a circuit diagram showing the 1st example of the composition of the subtraction amplifier in the analog-to-digital circuit of drawing 3.
[Drawing 19]It is a circuit diagram showing the 2nd example of the composition of the subtraction amplifier in the analog-to-digital circuit of drawing 3.
[Drawing 20]It is a circuit diagram showing other examples of the switch part of a switching

means.
[Drawing 21]It is the top view and sectional view showing the example of further others of the switch part of a switching means.
[Drawing 22]It is the top view and sectional view showing the example of further others of the switch part of a switching means.
[Drawing 23]It is a block diagram showing the conventional analog-to-digital circuit.
[Drawing 24]It is a figure for explaining operation of the circuit diagram showing the composition of the subtraction amplifier of the analog-to-digital circuit of drawing 23, and its subtraction amplifier.
[Drawing 25]It is a figure showing the composition of the sub A/D converter used in the analog-to-digital circuit of drawing 23.
[Drawing 26]It is a figure for explaining the analog to digital in a differential double end input and a single-ended input.
[Description of Notations]
1 Analog-to-digital circuit
3-6 The 1st step - the 4th step of circuit
9, 9a, and 9b Sub A/D converter
10 and 10b D/A converter
11, 13, and 13a Arithmetic amplifier
12 Subtractor circuit
14 14a Subtraction amplifier
VRT, VRT2, and VRT3 The high potential side reference voltage
VRB, VRB2, and VRB3 The low voltage side reference voltage
VRT1 Middle reference voltage
Sa, S1a, S1b, S24, S25, S26, S26, S28, S29, S30, and S31 Switch

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[Translation done.]

* NOTICES *

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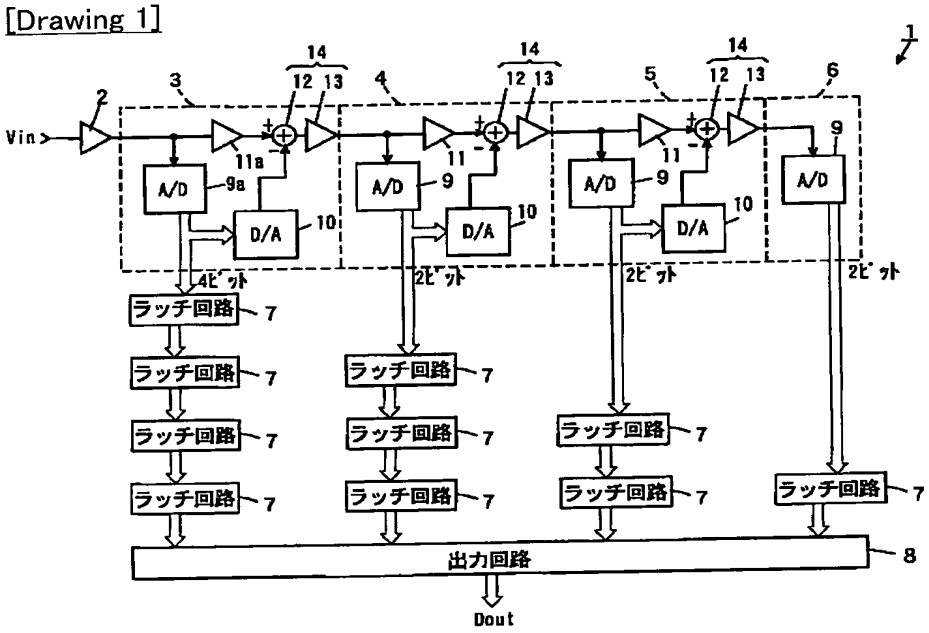
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

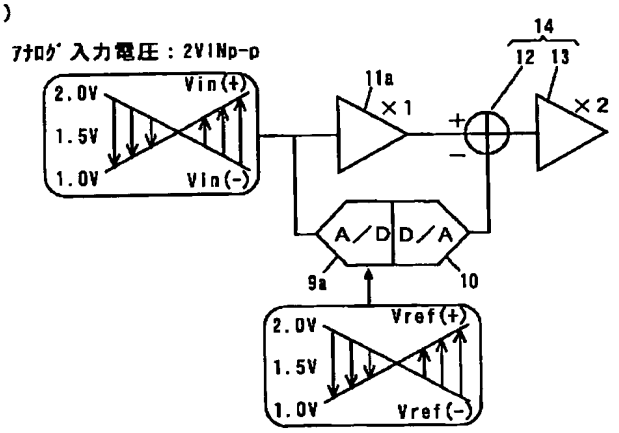
DRAWINGS

[Drawing 1]



[Drawing 2]

(a)



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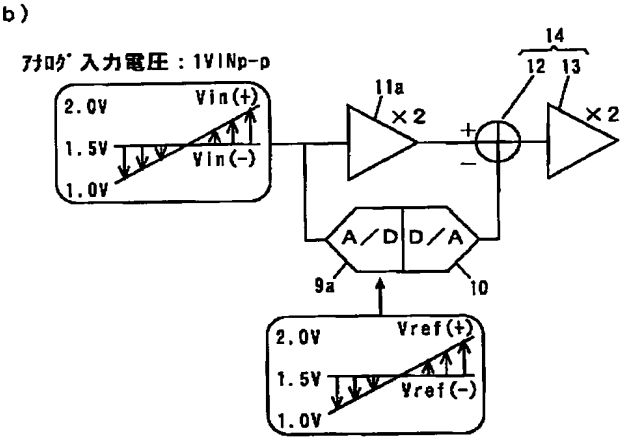
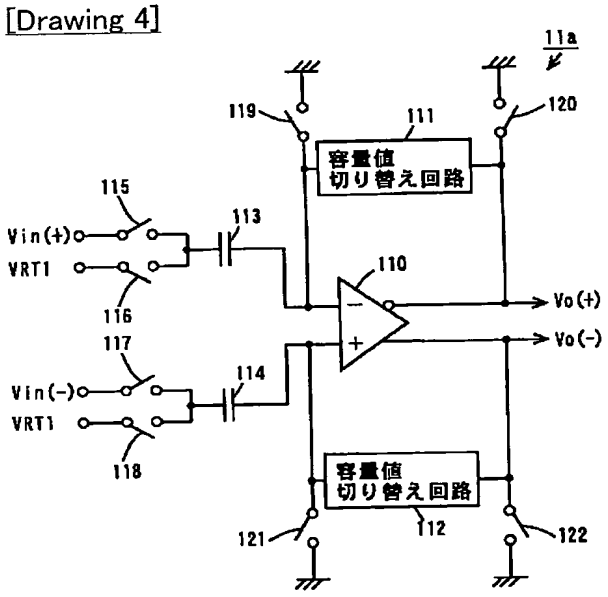
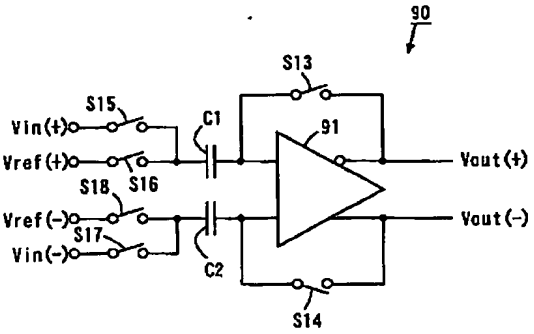


[Drawing 4]



[Drawing 13]



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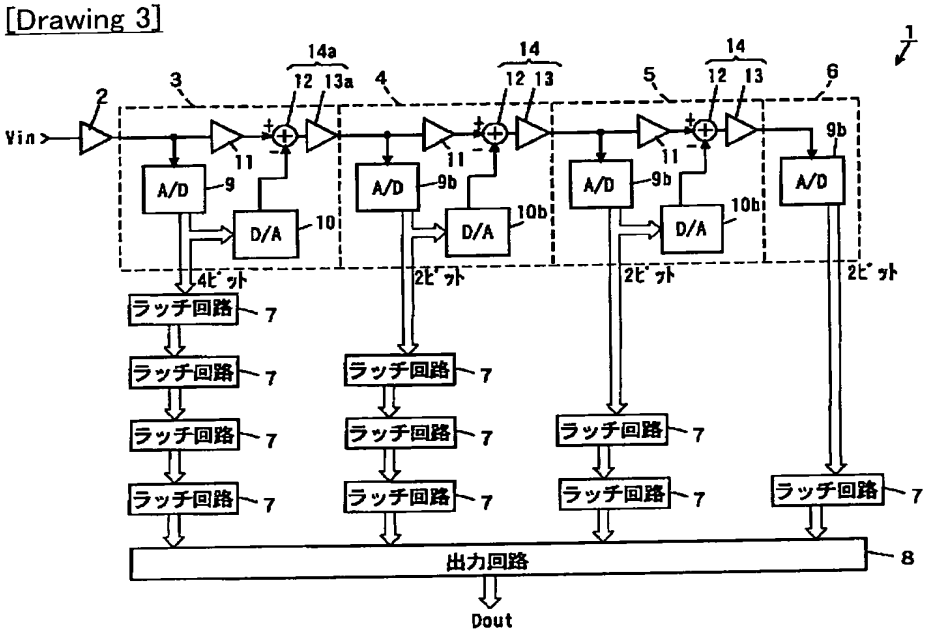

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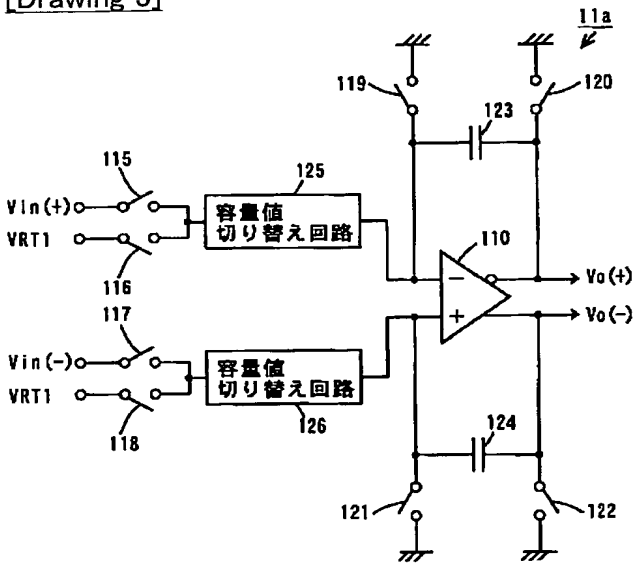

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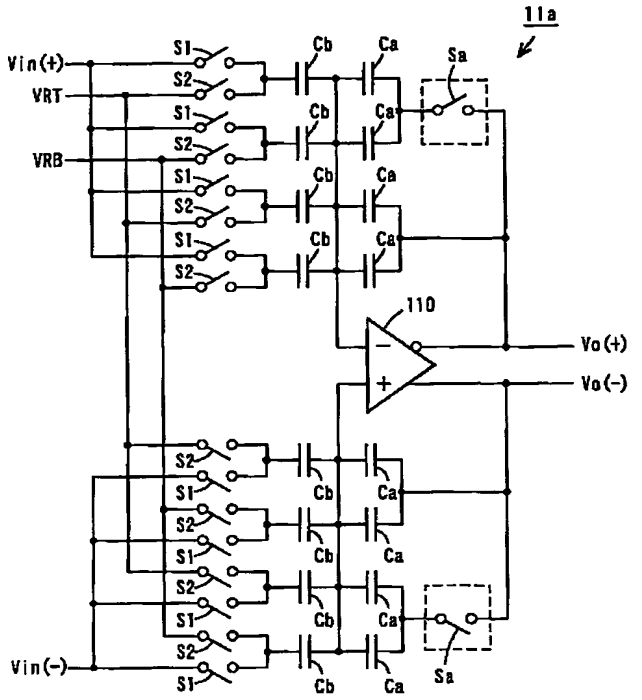
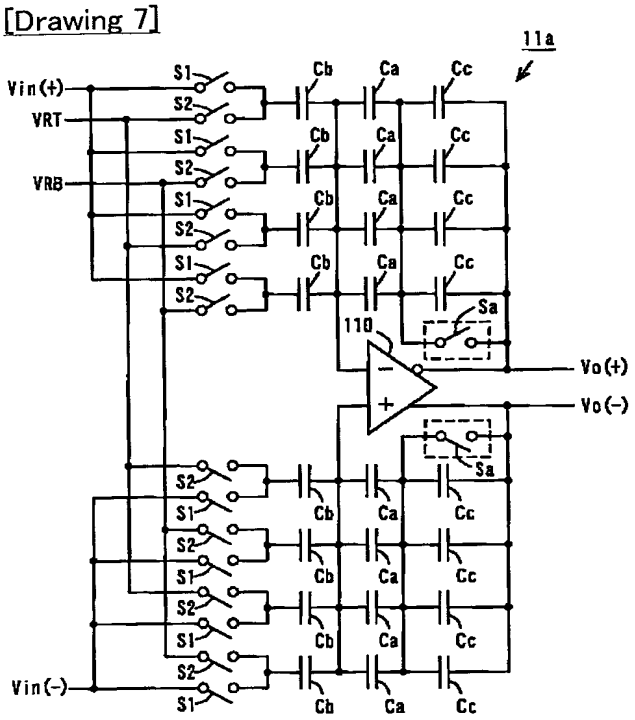


[Drawing 7]



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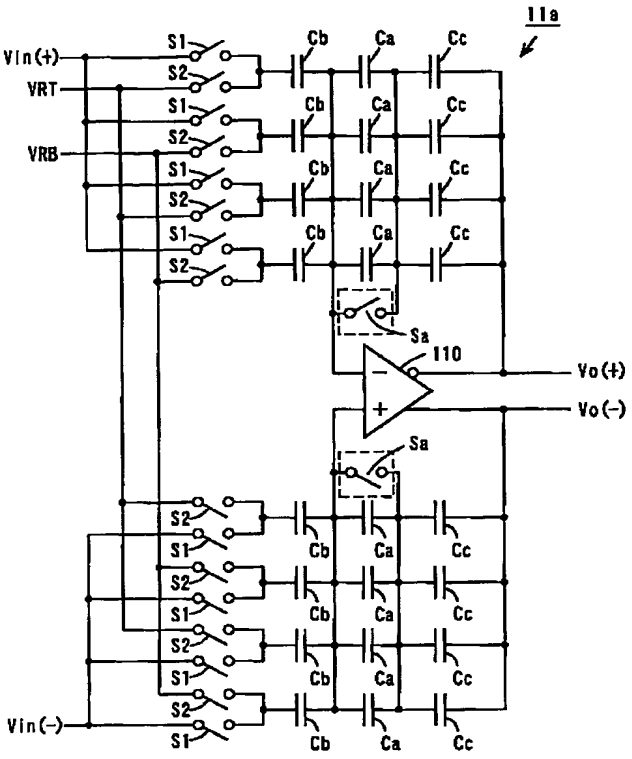

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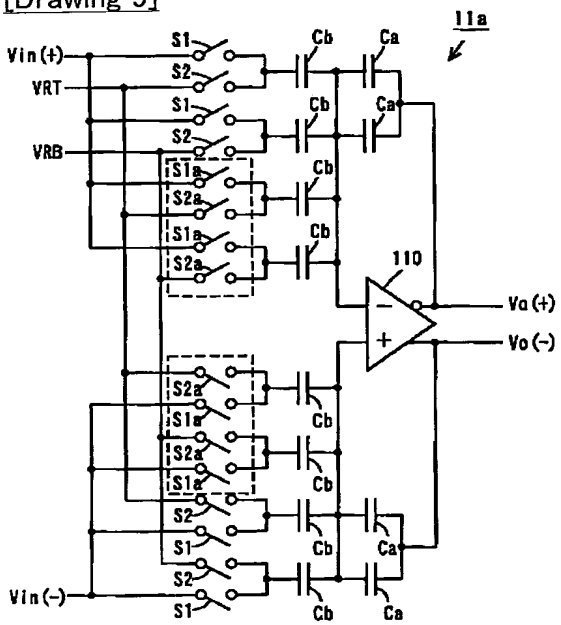
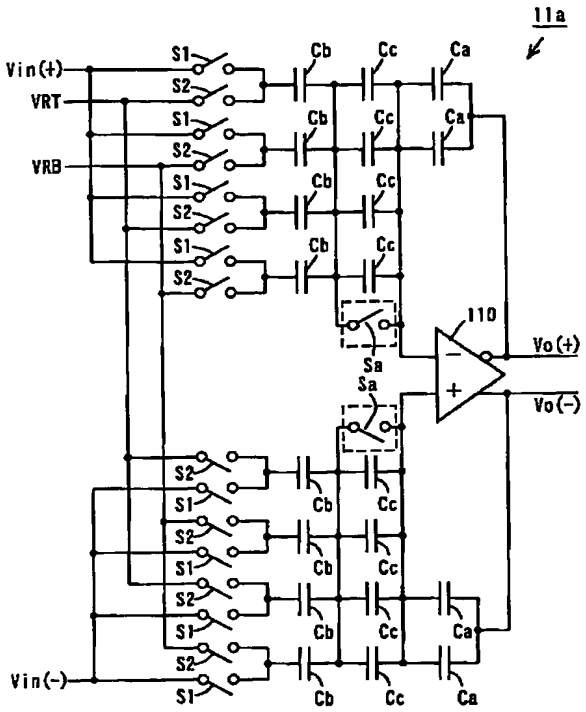
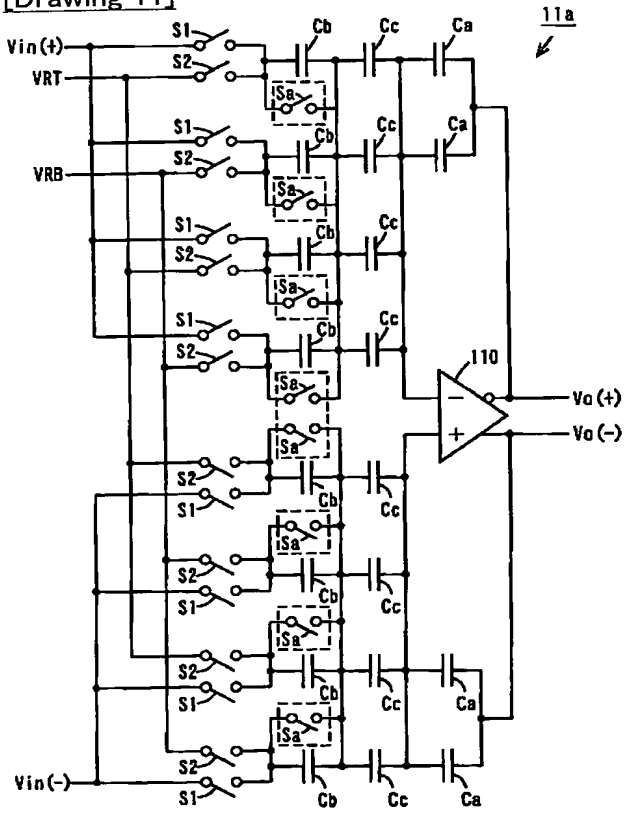


[Drawing 10]



[Drawing 11]



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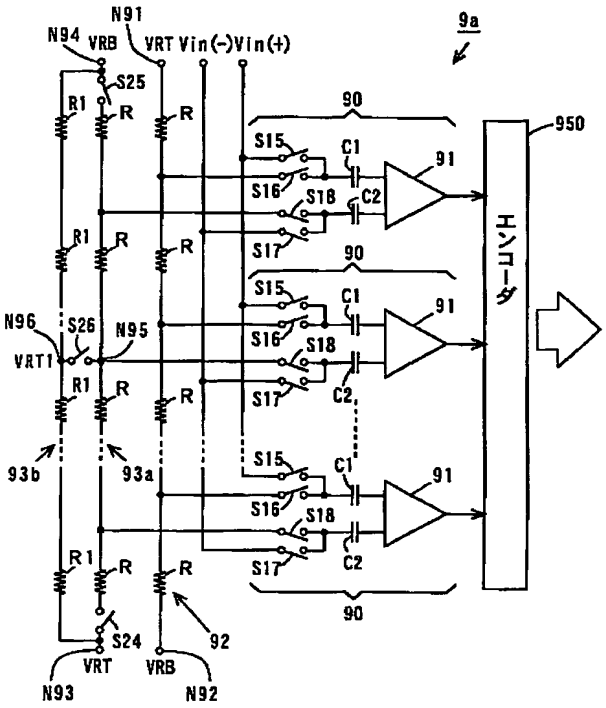
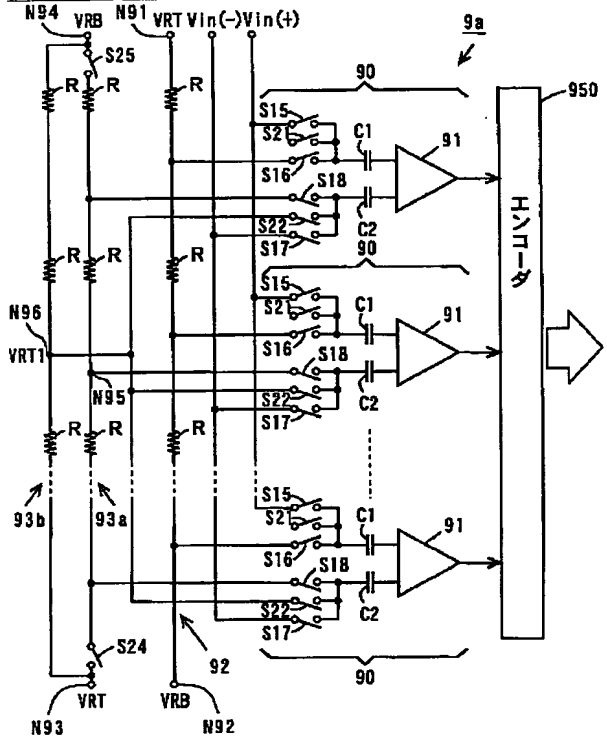
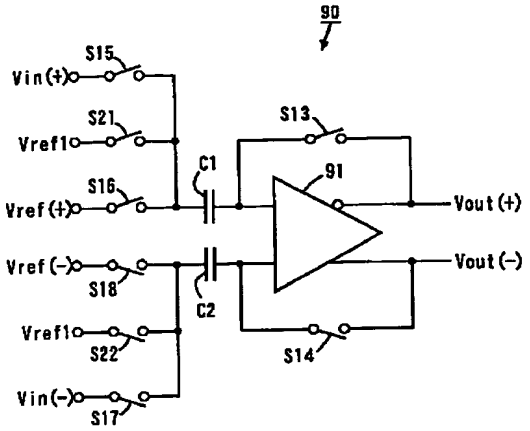


[Drawing 14]



[Drawing 15]



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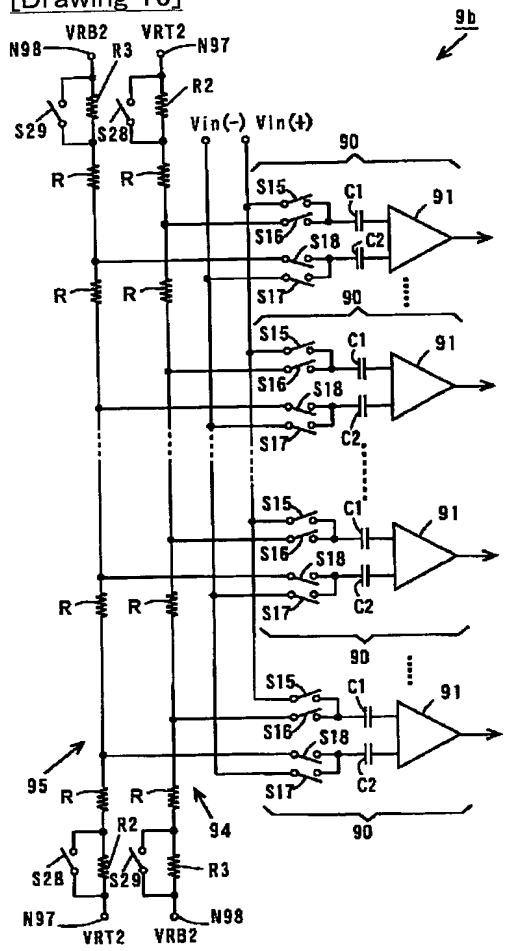

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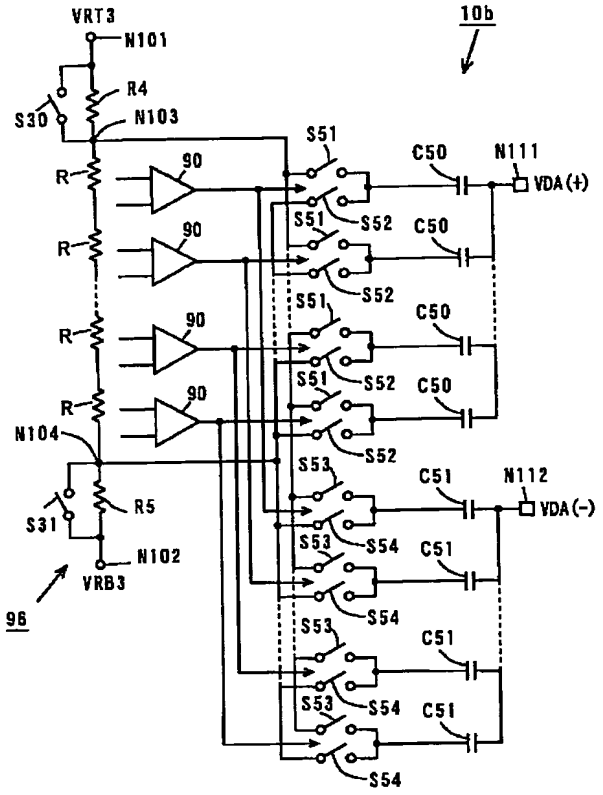

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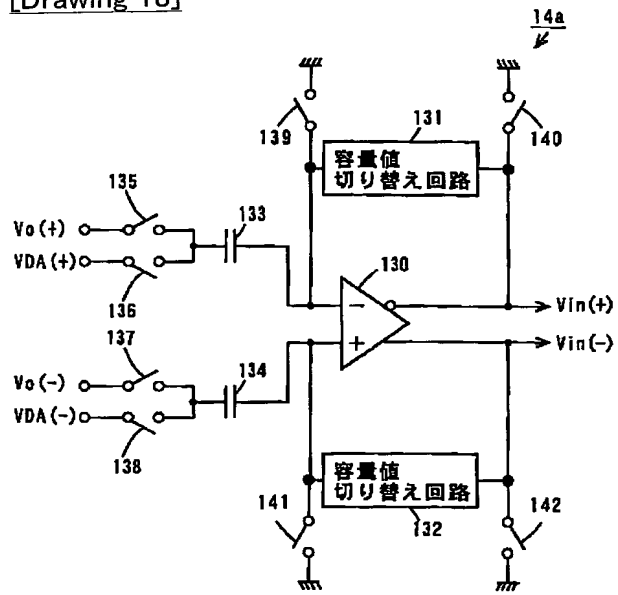

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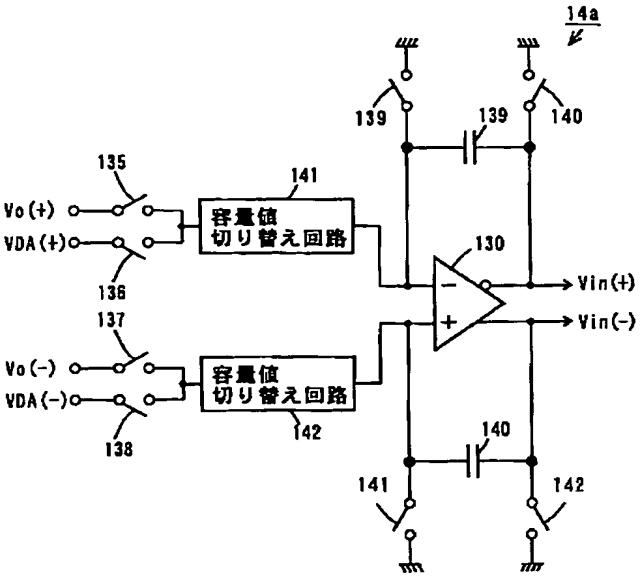
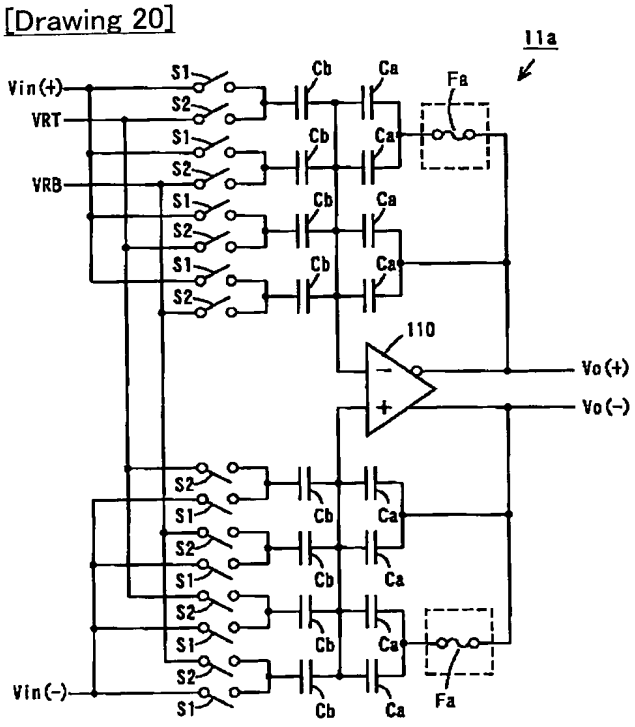


[Drawing 20]



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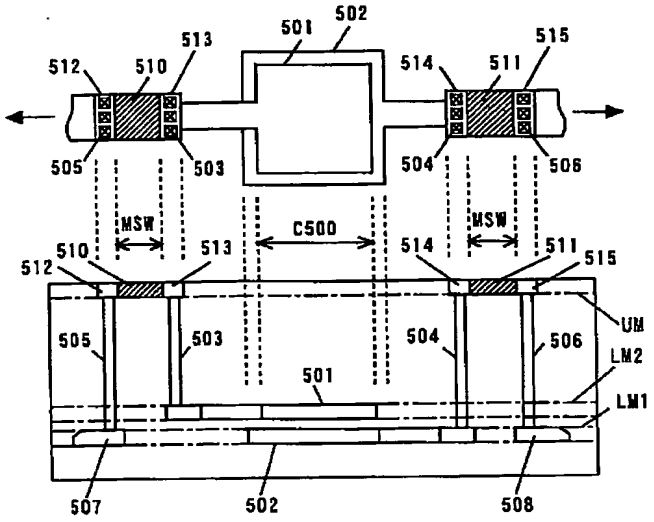

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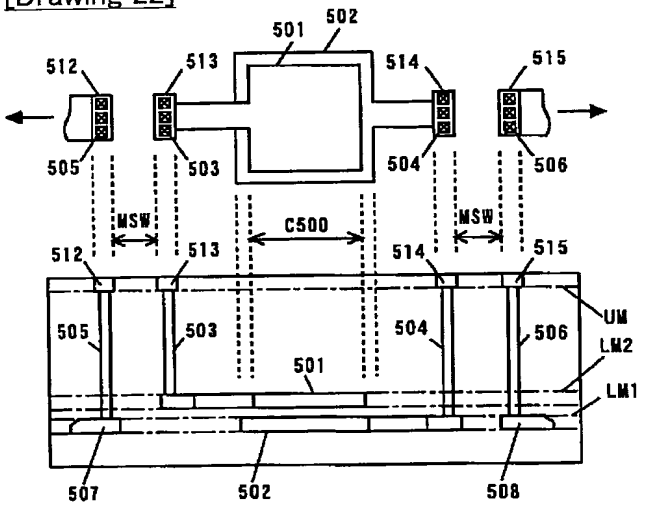

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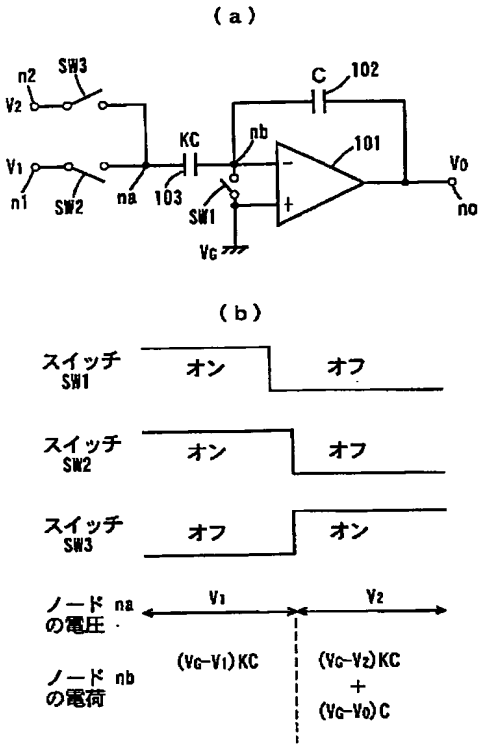

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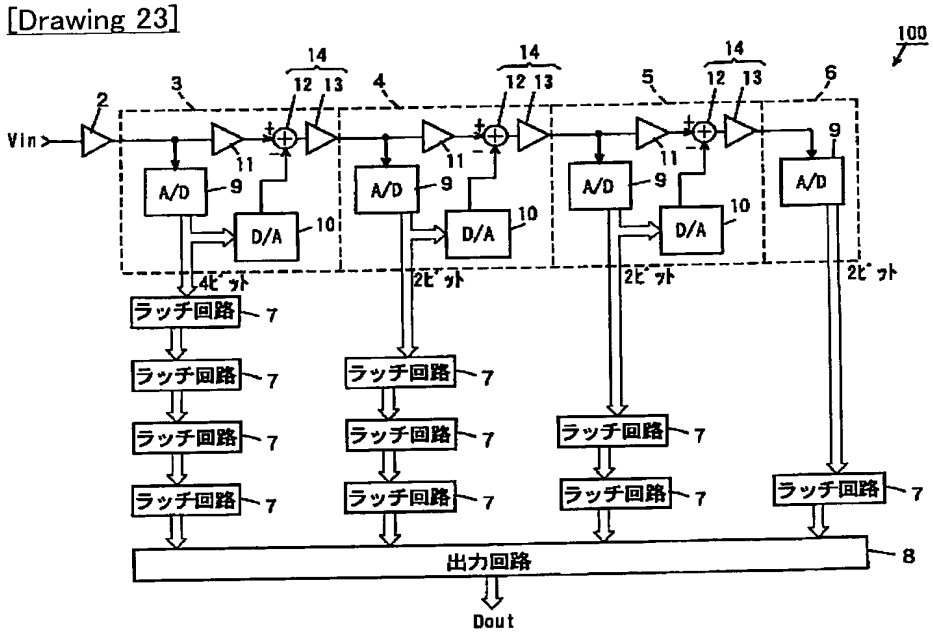

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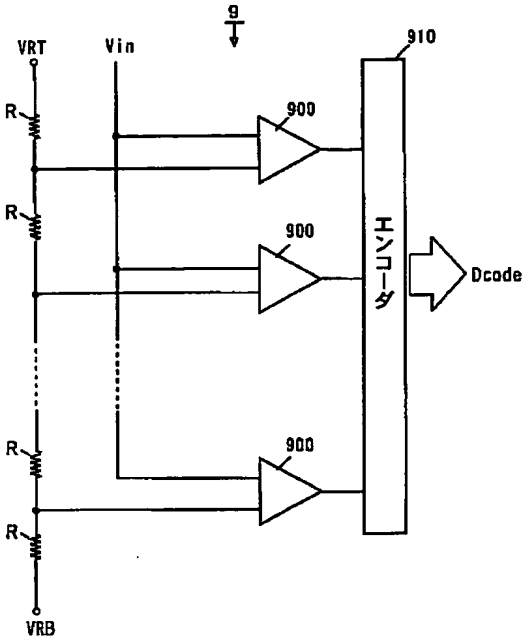

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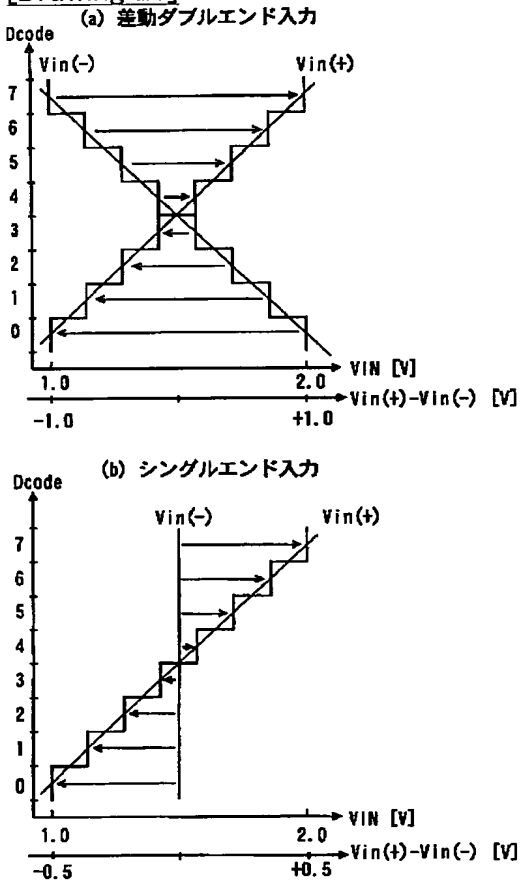

[Translation done.]

(19)日本国特許庁（ＪＰ）　(12) 公開特許公報（Ａ）　(11)特許出願公開番号
特開2003－188727
（P2003－188727A）
(43)公開日　平成15年７月４日(2003.7.4)

(51)Int.Cl.'	識別記号	ＦＩ	ﾃｰﾏｺｰﾄﾞ(参考)
Ｈ０３Ｍ　1/44		Ｈ０３Ｍ　1/44	５Ｊ０２２

審査請求　未請求　請求項の数15　ＯＬ　（全 27 頁）

(21)出願番号　特願2001－384369(P2001－384369)

(22)出願日　平成13年12月18日(2001.12.18)

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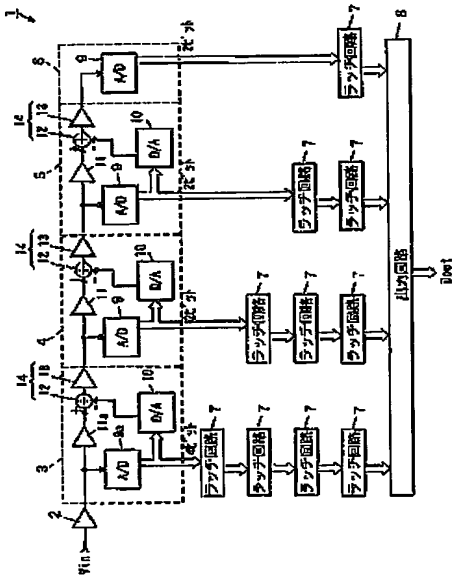
最終頁に続く

(54)【発明の名称】　アナログ－デジタル変換回路

(57)【要約】
【課題】　回路構成の再設計を行うことなくアナログ入力信号の電圧レンジの変更または差動ダブルエンド入力とシングルエンド入力との間の入力方式の変更を容易に行うことができるパイプライン型アナログ－デジタル変換回路を提供することである。
【解決手段】　アナログ入力信号の電圧レンジがＶＩＮ$_{0-0}$のときに、サブＡ／Ｄコンバータ９のフルスケールレンジはＶＩＮ$_{0-0}$に切り替えられ、演算増幅回路１１ａの利得は１倍に切り替えられる。アナログ入力信号の電圧レンジがＶＩＮ$_{0-0}$／２のときに、サブＡ／Ｄコンバータ９のフルスケールレンジはＶＩＮ$_{0-0}$／２に切り替えられ、演算増幅回路１１ａの利得は２倍に切り替えられる。



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【特許請求の範囲】

【請求項１】　複数段の回路からなる多段パイプライン構成を有し、

最終段の回路を除く各段の回路は、

入力されたアナログ信号をデジタル信号に変換するアナログ－デジタル変換器と、

前記アナログ－デジタル変換器から出力されるデジタル信号をアナログ信号に変換するデジタル－アナログ変換器と、

入力されるアナログ信号と前記デジタル－アナログ変換器から出力されるアナログ信号との差分を増幅する第１の演算増幅回路とを備え、

最終段の回路は、入力されたアナログ信号をデジタル信号に変換するアナログ－デジタル変換器を含み、

最終段の回路を除く少なくとも１段の回路が、フルスケールレンジを複数段に切り替える切り替え手段を有するアナログ－デジタル変換器、フルスケールレンジを複数段に切り替える切り替え手段を有するデジタル－アナログ変換器および利得を複数段に切り替える切り替え手段を有する第１の演算増幅回路のうち少なくとも１つを含み、および／または最終段の回路がフルスケールレンジを複数段に切り替える切り替え手段を有するアナログ－デジタル変換器を含むことを特徴とするアナログ－デジタル変換回路。

【請求項２】　最終段の回路を除く各段の回路は、入力されたアナログ信号を増幅して前記第１の演算増幅回路に与える第２の演算増幅回路をさらに含み、最終段の回路を除く少なくとも１段の回路の前記第２の演算増幅回路は、利得を複数段に切り替える切り替え手段を有することを特徴とする請求項１記載のアナログ－デジタル変換回路。

【請求項３】　最終段の回路を除く少なくとも１段の回路の前記第１の演算増幅回路は、利得を複数段に切り替える切り替え手段を有することを特徴とする請求項１または２記載のアナログ－デジタル変換回路。

【請求項４】　少なくとも１段の回路の前記アナログ－デジタル変換器は、フルスケールレンジを複数段に切り替える切り替え手段を有することを特徴とする請求項１～３のいずれかに記載のアナログ－デジタル変換回路。

【請求項５】　最終段の回路を除く少なくとも１段の回路の前記デジタル－アナログ変換器は、フルスケールレンジを複数段に切り替える切り替え手段を有することを特徴とする請求項１～４のいずれかに記載のアナログ－デジタル変換回路。

【請求項６】　前記少なくとも１段の回路の前記第２の演算増幅回路は、入力容量、帰還容量および演算増幅器を有し、入力されたアナログ信号を前記入力容量の値および前記帰還容量の値により定まる利得で増幅し、

前記切り替え手段は、前記入力容量の値および前記帰還容量の値の少なくとも一方を可変に設定する可変部を含むことを特徴とする請求項２記載のアナログ－デジタル変換回路。

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【請求項７】　前記可変部は、前記入力容量または前記帰還容量の一部を切り離された状態または短絡された状態に切り替える切り替え部を含むことを特徴とする請求項６記載のアナログ－デジタル変換回路。

【請求項８】　前記少なくとも１段の回路の前記第１の演算増幅回路は、入力容量、帰還容量および演算増幅器を有し、入力されたアナログ信号を前記入力容量の値および前記帰還容量の値により定まる利得で増幅し、

前記切り替え手段は、前記入力容量の値および前記帰還容量の値の少なくとも一方を可変に設定する可変部を含むことを特徴とする請求項３記載のアナログ－デジタル変換回路。

【請求項９】　前記可変部は、前記入力容量または前記帰還容量の一部を切り離された状態または短絡された状態に切り替える切り替え部を含むことを特徴とする請求項８記載のアナログ－デジタル変換回路。

【請求項１０】　前記帰還容量は、前記演算増幅器の入力端子と出力端子との間に並列または直列に設けられた第１および第２の容量を含み、

前記切り替え部は、前記第２の容量に直列または並列に接続されたことを特徴とする請求項９記載のアナログ－デジタル変換回路。

【請求項１１】　前記切り替え部は、前記演算増幅器の出力端子に接続されたことを特徴とする請求項１０記載のアナログ－デジタル変換回路。

【請求項１２】　前記入力容量は、前記演算増幅器の入力端子に並列または直列に設けられた第１および第２の容量を含み、

前記切り替え部は、前記第２の容量に直列または並列に接続されたことを特徴とする請求項９記載のアナログ－デジタル変換回路。

【請求項１３】　前記切り替え部前は、前記第２の容量の入力側に接続されたことを特徴とする請求項１２記載のアナログ－デジタル変換回路。

【請求項１４】　少なくとも１段の回路の前記アナログ－デジタル変換器は、複数の基準電圧を発生する基準電圧発生回路と、前記基準電圧発生回路により発生された複数の基準電圧を入力されたアナログ信号と比較する複数の比較器とを含み、

前記切り替え手段は、前記基準電圧発生回路により発生される複数の基準電圧を可変に設定する可変部を含むことを特徴とする請求項４記載のアナログ－デジタル変換回路。

【請求項１５】　最終段の回路を除く少なくとも１段の回路の前記デジタル－アナログ変換器は、基準電圧を発生する基準電圧発生回路と、共通の端子に接続される複数の容量と、前記基準電圧発生回路と前記複数の容量との間に接続され、入力されるデジタル信号に応じて前記

基準電圧発生回路により発生された基準電圧を前記複数の容量にそれぞれ与える複数のスイッチとを含み．
前記切り替え手段は、前記基準電圧発生回路により発生される基準電圧を可変に設定する可変部を含むことを特徴とする請求項５記載のアナログ－デジタル変換回路。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は．多段パイプライン（ステップフラッシュ）構成を有するアナログ－デジタル変換回路に関する。

【０００２】

【従来の技術】近年、ビデオ信号のデジタル処理技術の進歩に伴い、ビデオ信号処理用のアナログ－デジタル変換回路（Ａ／Ｄコンバータ）の需要が大きくなっている。ビデオ信号処理用のアナログ－デジタル変換回路には高速変換動作が要求されるため、従来、２ステップフラッシュ（２ステップパラレル）方式が広く用いられていた。

【０００３】しかし、変換ビット数の増大に伴い．２ステップフラッシュ方式では十分な変換精度が得られなくなってきたため．多段パイプライン（ステップフラッシュ）構成を有するアナログ－デジタル変換回路が開発された。

【０００４】図２３は特開平１１－８８１７２号公報に開示された従来のアナログ－デジタル変換回路を示すブロック図である。図２３のアナログ－デジタル変換回路１００は、１０ビット４段パイプライン構成を有する。

【０００５】図２３において、アナログ－デジタル変換回路１００は．サンプルホールド回路２、１段目～４段目の回路３～６．複数のラッチ回路７および出力回路８から構成されている。

【０００６】１段目（初段）～３段目の回路３、４，５は．サブＡ／Ｄコンバータ９、Ｄ／Ａコンバータ１０、演算増幅回路１１、減算回路１２および演算増幅回路１３を備える。減算回路１２および演算増幅回路１３が減算増幅回路１４を構成する。１段目の回路３内の演算増幅回路１１の利得は１であり、１段目の回路３内の演算増幅回路１３および２段目および３段目の回路４．５内の演算増幅回路１１，１３の利得は２である。４段目（最終段）の回路６は、サブＡ／Ｄコンバータ９のみを＊備える。

【０００７】１段目の回路３は４ビット構成、２～４段目の回路４～６はそれぞれ２ビット構成である。１～３段目の回路３～５において．サブＡ／Ｄコンバータ９およびＤ／Ａコンバータ１０のビット数（ビット構成）は同じに設定されている。

【０００８】

【発明が解決しようとする課題】ここで、上記のアナログ－デジタル変換回路１００では、アナログ入力信号Ｖｉｎの電圧レンジをＶｉＮ$_{0-0}$とすると、１段目の回路３内のサブＡ／Ｄコンバータ９のフルスケールレンジはアナログ入力信号の電圧レンジＶｉＮ$_{0-0}$と等しい。２～４段目の回路４～６内のサブＡ／Ｄコンバータ９のフルスケールレンジはそれぞれ１～３段目の回路３～５の減算増幅回路１４の出力電圧レンジＶＩＮ$_{0-0}$／８と等しい。

【０００９】また、１段目の回路３内のＤ／Ａコンバータ１０のフルスケールレンジはサブＡ／Ｄコンバータ９と同様にアナログ入力信号Ｖｉｎの電圧レンジＶＩＮ$_{0-0}$と等しい。２段目および３段目の回路４，５内のＤ／Ａコンバータ１０の電圧のフルスケールレンジは利得２を有する演算増幅回路１１の出力電圧レンジとの整合を取るためにサブＡ／Ｄコンバータ９のフルスケールレンジの２倍のＶＩＮ$_{0-0}$／４となる。

【００１０】次に、図２３のアナログ－デジタル変換回路１の動作を説明する。サンプルホールド回路２は、アナログ入力信号Ｖｉｎをサンプリングして一定時間保持する。サンプルホールド回路２から出力されたアナログ入力信号Ｖｉｎは、１段目の回路３へ転送される。

【００１１】１段目の回路３において．サブＡ／Ｄコンバータ９は、電圧レンジＶＩＮ$_{0-0}$のアナログ入力信号Ｖｉｎに対してアナログ－デジタル変換を行う。ここで．サブＡ／Ｄコンバータ９のフルスケールレンジは、上記のようにＶＩＮ$_{0-0}$である。サブＡ／Ｄコンバータ９のアナログ－デジタル変換結果であるデジタル出力（2^3，2^2，2^1，2^0）は、Ｄ／Ａコンバータ１０へ転送されるとともに、４つのラッチ回路７を介して出力回路８へ転送される。Ｄ／Ａコンバータ１０の正規出力電圧レンジは．次式のように表される。

【００１２】

（１段目の分解能－１）×（Ｄ／Ａコンバータ１０のフルスケールレンジ）／（１段目の分解能）

＝（2^4-1）×（ＶｉＮ$_{0-0}$）／2^4

＝１５ＶｉＮ$_{0-0}$／１６

一方．演算増幅回路１１は．アナログ入力信号Ｖｉｎをサンプリングして増幅および保持する。演算増幅回路１※　※１の出力電圧レンジは、次式のように表される。

【００１３】

（アナログ入力信号Ｖｉｎの電圧レンジＶｉＮ$_{0-0}$）×（演算増幅回路１１の利得）

＝ＶｉＮ$_{0-0}$×１

＝ＶｉＮ$_{0-0}$

減算増幅回路１４は、演算増幅回路１１から出力されたアナログ入力信号Ｖｉｎと Ｄ／Ａコンバータ１０のＤ／Ａ変換結果とを減算して増幅する。減算増幅幅回路１４の出力は、２段目の回路４へ転送される。１段目の減算＊

（（演算増幅回路１１の出力電圧レンジ）－（Ｄ／Ａコンバータ１０の正規出力電圧レンジ））×（減算増幅回路１４の利得）

＝（（ＶｉＮ$_{0-0}$）－（１５ＶｉＮ$_{0-0}$／１６））×２

＝ＶｉＮ$_{0-0}$／８

２段目の回路４においては、サブＡ／Ｄコンバータ９が、１段目の回路３の減算増幅回路１４の出力に対してＡ／Ｄ変換を行う。サブＡ／Ｄコンバータ９のＡ／Ｄ変換結果は、Ｄ／Ａコンバータ１０へ転送されるとともに、３つのラッチ回路７を介して出力回路８へ転送され※

（２段目の分解能－１）×（Ｄ／Ａコンバータ１０のフルスケールレンジ）／（２段目の分解能）

＝（２^{2}－１）×（ＶｉＮ$_{0-0}$／４）／２^{2}

＝３ＶｉＮ$_{0-0}$／１６

一方、演算増幅回路１１は、１段目の回路３の減算増幅回路１３の出力を増幅する。演算増幅回路１１の出力★

（１段目の減算増幅回路１４の出力電圧レンジ）×（演算増幅回路１１の利得）

＝（ＶｉＮ$_{0-0}$／８）×２

＝ＶｉＮ$_{0-0}$／４

減算増幅回路１４は、演算増幅回路１１の出力とＤ／Ａコンバータ１０のＤ／Ａ変換結果とを減算して増幅する。減算増幅回路１４の出力は、３段目の回路５へ転送☆

（（演算増幅回路１１の出力電圧レンジ）－（Ｄ／Ａコンバータ１０の正規出力電圧レンジ））×（減算増幅回路１４の利得）

＝（（ＶｉＮ$_{0-0}$／４）－（３ＶＩＮ$_{0-0}$／１６））×２

＝ＶｉＮ$_{0-0}$／８

３段目の回路５においては、２段目の回路３の減算増幅回路１４の出力に対して２段目の回路４と同様の動作が行われる。それにより、３段目の回路５から中下位２ビットのデジタル出力（２^{1}，２^{0}）が得られる。各部の出力電圧レンジは２段目の回路４と同様である。

【００１８】４段目の回路６においては、３段目の回路５の減算増幅回路１４の出力に対してサブＡ／Ｄコンバータ９がＡ／Ｄ変換を行い、下位２ビットのデジタル出力（２^{1}，２^{0}）が得られる。

【００１９】１段目～４段目の回路３～６のデジタル出力は、各ラッチ回路７を経て同時に出力回路８に到達する。すなわち、各ラッチ回路７は各回路３～６のデジタル出力の同期をとるために設けられている。

【００２０】出力回路８は、アナログ入力信号Ｖｉｎの１０ビットのデジタル出力Ｄｏｕｔを必要な場合はデジタル補正処理後パラレル出力する。

【００２１】このようにして、変換ビット数が増大し、電源電圧の減少に伴いＬＳＢ（Least Significant Bit）が小さくなっても、サブＡ／Ｄコンバータ９の分解能を向上させることができ、十分な変換精度が得られる。

＊増幅回路１４の出力電圧レンジは、次式のように表される。

【００１４】

※る。これにより、２段目の回路４から中上位２ビットのデジタル出力（２^{1}，２^{0}）が得られる。Ｄ／Ａコンバータ１０の正規出力電圧レンジは、次式のように表される。

【００１５】

★圧レンジは次式のように表される。

【００１６】

☆される。２段目の減算増幅回路１４の出力電圧のレンジは、次式のように表される。

【００１７】

【００２２】図２４（ａ）は図２３のアナログ－デジタル変換回路の減算増幅回路の構成を示す回路図、図２４（ｂ）は図２４（ａ）の減算増幅回路の動作を説明するための図である。

【００２３】図２４において、演算増幅器１０１の反転入力端子はノードｎｂに接続され、非反転入力端子は接地されている。また、演算増幅器１０１の出力端子はノードｎｏに接続されるとともにコンデンサ１０２を介して反転入力端子に接続されている。演算増幅器１の反転入力端子と非反転入力端子との間にはスイッチＳＷ１が接続され、ノードｎｂとノードｎａとの間にコンデンサ１０３が接続されている。ノードｎａは、スイッチＳＷ２を介してノードｎ１に接続され、かつスイッチＳＷ３を介してノードｎ２に接続されている。これらのスイッチＳＷ２，ＳＷ３は、通常ＣＭＯＳ（相補型金属酸化物半導体）電界効果トランジスタからなるＣＭＯＳスイッチにより構成される。

【００２４】ノードｎ１に電圧Ｖ$_{1}$が入力され、ノードｎ２に電圧Ｖ$_{2}$が入力され、ノードｎｏから電圧Ｖ$_{o}$が

出力される。

【００２５】ここで、図２４（ｂ）を参照しながら図２４（ａ）の減算増幅回路の動作を説明する。なお、コンデンサ１０１の容量値をＣとし、コンデンサ１０３の容量値をＫＣとし、接地電位をV_cとする。Ｋは定数である。

【００２６】まず、スイッチＳＷ１およびスイッチＳＷ２をオンにし、スイッチＳＷ３をオフにする。それにより、ノードｎａの電圧はV_1となる。また、ノードｎｏの電圧は０となる。このとき、ノードｎｂの電荷Ｑａは次式のようになる。

【００２７】$Q_a = (V_c - V_1) KC$

次に、スイッチＳＷ１をオフにした後、スイッチＳＷ２をオフにし、かつスイッチＳＷ３をオンにする。それにより、ノードｎａの電圧はV_2となる。また、ノードｎｏの電圧はV_oとなる。このとき、ノードｎｂは仮想接地するため、ノードｎｂの電荷Ｑｂは次式のようになる。

【００２８】

$Q_b = (V_c - V_2) KC + (V_c - V_o) C$

ノードｎｂには電荷が抜け出る経路がないので、電荷保存則により$Q_a = Q_b$となる。したがって、次式が成立する。

【００２９】$(V_c - V_1) KC = (V_c - V_2) KC + (V_c - V_o) C$

上式から、ノードｎｏの電圧V_oは次式のようになる。

【００３０】$V_o = V_c + (V_1 - V_2) K$

このようにして、電圧V_1から電圧V_2が減算され、その減算値がＫ倍に増幅される。

【００３１】したがって、減算増幅回路は電圧V_1と電圧V_2との差をコンデンサ１０３とコンデンサ１０２との容量比で決まる利得によって出力する機能を有する。例えば、$KC = C$（$K = 1$）に設定することにより、減算増幅回路に利得１倍のサンプルホールド機能を持たせることとなる。

【００３２】図２５は図２３のアナログ－デジタル変換回路において用いられるサブＡ／Ｄコンバータの構成を示す図である。

【００３３】図２５の並列型アナログ－デジタルコンバータ９において、複数のコンパレータ９００が配置されている。複数のコンパレータ９００の一方の入力端子にはアナログ入力電圧Ｖｉｎが与えられ、他方の入力端子には高電位側基準電圧ＶＲＴと低電位側基準電圧ＶＲＢとの間の電圧を複数の抵抗Ｒで分圧することにより得られる基準電圧がそれぞれ与えられる。各コンパレータ９００は、一方の入力端子の電圧と他方の入力端子の電圧とを比較する。複数のコンパレータ９００の比較結果をエンコーダ９１０によってエンコードすることにより、デジタルコードＤｃｏｄｅを得ることができる。

【００３４】ところで、アナログ－デジタル変換回路に

与えるアナログ入力信号の電圧レンジを変更する場合、またはアナログ－デジタル変換回路に与えるアナログ入力信号の方式を差動ダブルエンド入力とシングルエンド入力とで変更する場合には、アナログ－デジタル変換回路の仕様を変更する必要がある。

【００３５】ここで、差動ダブルエンド入力およびシングルエンド入力について説明する。図２６（ａ）、（ｂ）は差動ダブルエンド入力およびシングルエンド入力におけるアナログ－デジタル変換を説明するための図である。横軸はアナログ入力電圧ＶＩＮを示し、縦軸は出力されたデジタルコードＤｃｏｄｅを示す。

【００３６】図２６（ａ）に示すように、差動ダブルエンド入力時においては、アナログ入力信号Ｖｉｎの正側アナログ入力電圧Ｖｉｎ（＋）および負側アナログ入力電圧Ｖｉｎ（－）が相補的に変化する。それにより、正側アナログ入力電圧Ｖｉｎ（＋）と負側アナログ入力電圧Ｖｉｎ（－）との差分がアナログ入力信号Ｖｉｎの電圧レンジ$V_{IN_{-p-p}}$となる。

【００３７】したがって、図２６（ａ）に示すように、正側アナログ入力電圧Ｖｉｎ（＋）が１．０Ｖから２．０の範囲で変化し、負側アナログ入力電圧Ｖｉｎ（－）が２．０Ｖから１．０Ｖの範囲で変化する場合、アナログ入力信号Ｖｉｎの電圧レンジはＶｉｎ（＋）－Ｖｉｎ（－）の演算から２．０Ｖとなる。

【００３８】一方、図２６（ｂ）に示すように、シングルエンド入力時においては、正側アナログ入力電圧Ｖｉｎ（＋）のみが変化する。それにより、正側アナログ入力電圧Ｖｉｎ（＋）の電圧レンジがアナログ入力信号Ｖｉｎの電圧レンジとなる。

【００３９】したがって、図２６（ｂ）に示すように、正側アナログ入力電圧Ｖｉｎ（＋）が１．０Ｖから２．０Ｖの範囲で変化する場合、アナログ入力信号の電圧レンジは１．０Ｖとなる。

【００４０】すなわち、差動ダブルエンド入力方式のアナログ入力信号Ｖｉｎの電圧レンジを$2V_{IN_{-p-p}}$とすると、シングルエンド入力方式のアナログ入力信号Ｖｉｎの電圧レンジは$V_{IN_{-p-p}}$となる。

【００４１】このように、差動ダブルエンド入力方式とシングルエンド入力方式とでは、各アナログ入力電圧の変化の範囲が同じであっても、アナログ入力信号の電圧レンジが異なることになる。

【００４２】上記の従来のアナログ－デジタル変換回路では、アナログ入力信号の電圧レンジの変更を行う場合、またはアナログ入力信号の入力方式の変更を行う場合に、回路構成を再設計する必要がある。

【００４３】本発明の目的は、回路構成の再設計を行うことなくアナログ入力信号の電圧レンジの変更または差動ダブルエンド入力とシングルエンド入力との間の入力方式の変更を容易に行うことができるパイプライン型アナログ－デジタル変換回路を提供することである。

【００４４】
【課題を解決するための手段および発明の効果】（１）第１の発明
第１の発明に係るアナログ－デジタル変換回路は，複数段の回路からなる多段パイプライン構成を有し，最終段の回路を除く各段の回路は，入力されたアナログ信号をデジタル信号に変換するアナログ－デジタル変換器と，アナログ－デジタル変換器から出力されるデジタル信号をアナログ信号に変換するデジタル－アナログ変換器と，入力されるアナログ信号とデジタル－アナログ変換器から出力されるアナログ信号との差分を増幅する第１の演算増幅回路とを備え，最終段の回路は，入力されたアナログ信号をデジタル信号に変換するアナログ－デジタル変換器を含み，最終段の回路を除く少なくとも１段の回路が，フルスケールレンジを複数段に切り替える切り替え手段を有するアナログ－デジタル変換器，フルスケールレンジを複数段に切り替える切り替え手段を有するデジタル－アナログ変換器および利得を複数段に切り替える切り替え手段を有する第１の演算増幅回路のうち少なくとも１つを含み，および／または最終段の回路がフルスケールレンジを複数段に切り替える切り替え手段を有するアナログ－デジタル変換器を含むものである。
【００４５】本発明に係るアナログ－デジタル変換回路においては，最終段の回路を除く少なくとも１段の回路が，フルスケールレンジを複数段に切り替える切り替え手段を有するアナログ－デジタル変換器，フルスケールレンジを複数段に切り替える切り替える切り替え手段を有するデジタル－アナログ変換器および利得を複数段に切り替える切り替え手段を有する第１の演算増幅回路のうち少なくとも１つを含み，および／または最終段の回路がフルスケールレンジを複数段に切り替える切り替え手段を有するアナログ－デジタル変換器を含むので，アナログ－デジタル変換回路のフルスケールレンジ，デジタル－アナログ変換器のフルスケールレンジおよび第１の演算増幅回路の利得のうち少なくとも１つを切り替えることができる。
【００４６】それにより，差動ダブルエンド入力方式をシングルエンド入力方式に変更することによりアナログ入力信号の電圧レンジが変更されても，回路構成の再設計が不要となる。また，シングルエンド入力のアナログ入力信号の電圧レンジを変更する場合または差動ダブルエンド入力のアナログ入力信号の電圧レンジを変更する場合にも，回路構成の再設計が不要となる。
【００４７】したがって，回路構成の再設計を行うことなくアナログ入力信号の電圧レンジの変更または差動ダブルエンド入力とシングルエンド入力との間の入力方式の変更を容易に行うことができる。
【００４８】その結果，アナログ－デジタル変換回路の開発期間の短縮化を図ることができるとともに，電圧レンジの最適化を最適化することにより低消費電力化を容易に行うことができる。
【００４９】（２）第２の発明
第２の発明に係るアナログ－デジタル変換回路は，第１の発明に係るアナログ－デジタル変換回路の構成において，最終段の回路を除く各段の回路は，入力されたアナログ信号を増幅して第１の演算増幅回路に与える第２の演算増幅回路をさらに含み，最終段の回路を除く少なくとも１段の回路の第２の演算増幅回路は，利得を複数段に切り替える切り替え手段を有するものである。
【００５０】この場合，少なくとも１段の回路の第２の演算増幅回路の利得を複数段に切り替えることにより，回路構成の再設計を行うことなくアナログ入力信号の電圧レンジの変更または差動ダブルエンド入力とシングルエンド入力との間の入力方式の変更を容易に行うことが可能となる。
【００５１】（３）第３の発明
第３の発明に係るアナログ－デジタル変換回路は，第１または第２の発明に係るアナログ－デジタル変換回路の構成において，最終段の回路を除く少なくとも１段の回路の第１の演算増幅回路は，利得を複数段に切り替える切り替え手段を有するものである。
【００５２】この場合，少なくとも１段の回路の第１の演算増幅回路の利得を複数段に切り替えることにより，回路構成の再設計を行うことなくアナログ入力信号の電圧レンジの変更または差動ダブルエンド入力とシングルエンド入力との間の入力方式の変更を容易に行うことが可能となる。
【００５３】（４）第４の発明
第４の発明に係るアナログ－デジタル変換回路は，第１～第３のいずれかの発明に係るアナログ－デジタル変換回路の構成において，少なくとも１段の回路のアナログ－デジタル変換器は，フルスケールレンジを複数段に切り替える切り替え手段を有するものである。
【００５４】この場合，少なくとも１段の回路のアナログ－デジタル変換器のフルスケールレンジを複数段に切り替え可能とることにより，回路構成の再設計を行うことなくアナログ入力信号の電圧レンジの変更または差動ダブルエンド入力とシングルエンド入力との間の入力方式の変更を容易に行うことが可能となる。
【００５５】（５）第５の発明
第５の発明に係るアナログ－デジタル変換回路は，第１～第４のいずれかの発明に係るアナログ－デジタル変換回路の構成において，最終段の回路を除く少なくとも１段の回路のデジタル－アナログ変換器は，フルスケールレンジを複数段に切り替える切り替え手段を有するものである。
【００５６】この場合，少なくとも１段の回路のデジタル－アナログ変換器のフルスケールレンジを複数段に切り替えることにより，回路構成の再設計を行うことなくアナログ入力信号の電圧レンジの変更または差動ダブル

エンド入力とシングルエンド入力との間の入力方式の変更を容易に行うことが可能となる。

【００５７】（６）第６の発明

第６の発明に係るアナログ－デジタル変換回路は、第２の発明に係るアナログ－デジタル変換回路の構成において、少なくとも１段の回路の第２の演算増幅回路は、入力容量、帰還容量および演算増幅器を有し、入力されたアナログ信号を入力容量の値および帰還容量の値により定まる利得で増幅し、切り替え手段は、入力容量の値および帰還容量の値の少なくとも一方を可変に設定する可変部を含むものである。

【００５８】この場合、入力されたアナログ信号が入力容量の値および帰還容量の値により定まる利得で増幅される。したがって、演算増幅器の入力容量の値および帰還容量の値の少なくとも一方を変更することにより、第２の演算増幅回路の利得を容易に切り替えることができる。

【００５９】（７）第７の発明

第７の発明に係るアナログ－デジタル変換回路は、第６の発明に係るアナログ－デジタル変換回路の構成において、可変部は、入力容量または帰還容量の一部を切り離された状態または短絡された状態に切り替える切り替え部を含むものである。

【００６０】この場合、切り替え部により入力容量または帰還容量の一部を切り離された状態または短絡された状態に切り替えることにより、演算増幅器の入力容量または帰還容量を変更することができる。それにより、第２の演算増幅回路の利得を容易に切り替えることができる。

【００６１】（８）第８の発明

第８の発明に係るアナログ－デジタル変換回路は、第３の発明に係るアナログ－デジタル変換回路の構成において、少なくとも１段の回路の第１の演算増幅回路は、入力容量、帰還容量および演算増幅器を有し、入力されたアナログ信号を入力容量の値および帰還容量の値により定まる利得で増幅し、切り替え手段は、入力容量の値および帰還容量の値の少なくとも一方を可変に設定する可変部を含むものである。

【００６２】この場合、入力されたアナログ信号が入力容量の値および帰還容量の値により定まる利得で増幅される。したがって、演算増幅器の入力容量の値および帰還容量の値の少なくとも一方を変更することにより、第１の演算増幅回路の利得を容易に切り替えることができる。

【００６３】（９）第９の発明

第９の発明に係るアナログ－デジタル変換回路は、第８の発明に係るアナログ－デジタル変換回路の構成において、可変部は、入力容量または帰還容量の一部を切り離された状態または短絡された状態に切り替える切り替え部を含むものである。

【００６４】この場合、切り替え部により入力容量または帰還容量の一部を切り離された状態または短絡された状態に切り替えることより、演算増幅器の入力容量または帰還容量を変更することができる。それにより、第１の演算増幅回路の利得を容易に切り替えることができる。

【００６５】（１０）第１０の発明

第１０の発明に係るアナログ－デジタル変換回路は、第９の発明に係るアナログ－デジタル変換回路の構成において、帰還容量は、演算増幅器の入力端子と出力端子との間に並列または直列に設けられた第１および第２の容量を含み、切り替え部は、第２の容量に直列または並列に接続されたものである。

【００６６】切り替え部を接続状態にすると、演算増幅器の入力端子と出力端子との間に第１および第２の容量が並列または直列に接続される。それにより、帰還容量が増加または減少する。また、切り替え部を遮断状態にすると、演算増幅器の入力端子と出力端子との間に第１の容量のみが接続される。それにより、帰還容量が減少または増加する。

【００６７】（１１）第１１の発明

第１１の発明に係るアナログ－デジタル変換回路は、第１０の発明に係るアナログ－デジタル変換回路の構成において、切り替え部は、演算増幅器の出力端子に接続されたものである。

【００６８】第２の容量が切り替え部よりも出力側に接続されている場合、切り替え部が遮断状態に設定されても、第２の容量の寄生容量が充電される。それにより、利得の設定時に、寄生容量を考慮する必要が生じ、寄生容量のばらつきにより利得がばらつくことになる。ここでは、切り替え部が第２の容量よりも出力側に接続されることにより、切り替え部が遮断状態に設定された場合に切り替え部により第２の容量が出力端子から寄生容量とともに切り離される。したがって、利得の設定時に第２の容量の寄生容量を考慮する必要がなくなり、寄生容量のばらつきによる利得のばらつきがなくなる。

【００６９】（１２）第１２の発明

第１２の発明に係るアナログ－デジタル変換回路は、第９の発明に係るアナログ－デジタル変換回路の構成において、入力容量は、演算増幅器の入力端子に並列または直列に設けられたものである。

【００７０】切り替え部を接続状態にすると、演算増幅器の入力端子に第１および第２の容量が並列または直列に接続される。それにより、入力容量が増加または減少する。また、切り替え部を遮断状態にすると、演算増幅器の入力端子に第１の容量のみが接続される。それにより、入力容量が減少または増加する。

【００７１】（１３）第１３の発明

第１３の発明に係るアナログ－デジタル変換回路は、第１２の発明に係るアナログ－デジタル変換回路の構成に

おいて、切り替え部は、第２の容量の入力側に接続されたものである。

【００７２】第２の容量が切り替え部よりも入力側に接続されている場合、切り替え部が遮断状態に設定されても、第２の容量の寄生容量が充電される。それにより、利得の設定時に、寄生容量を考慮する必要が生じ、寄生容量のばらつきにより利得がばらつくことになる。ここでは、切り替え部が第２の容量よりも入力側に接続されることにより、切り替え部が遮断状態に設定された場合に切り替え部により第２の容量が入力信号を受けるノードから寄生容量とともに切り離される。したがって、利得の設定時に第２の容量の寄生容量を考慮する必要がなくなり、寄生容量のばらつきによる利得のばらつきがなくなる。

【００７３】（１４）第１４の発明

第１４の発明に係るアナログ－デジタル変換回路は、第４の発明に係るアナログ－デジタル変換回路の構成において、少なくとも１段の回路のアナログ－デジタル変換器は、複数の基準電圧を発生する基準電圧発生回路と、基準電圧発生回路により発生された複数の基準電圧を入力されたアナログ信号と比較する複数の比較器とを含み、切り替え手段は、基準電圧発生回路により発生される複数の基準電圧を可変に設定する可変部を含むものである。

【００７４】この場合、基準電圧発生回路により発生される基準電圧を変更することにより、基準電圧の電圧レンジを変更することができる。それにより、アナログ－デジタル変換器のフルスケールレンジを容易に切り替えることができる。

【００７５】（１５）第１５の発明

第１５の発明に係るアナログ－デジタル変換回路は、第５の発明に係るアナログ－デジタル変換回路の構成において、最終段の回路を除く少なくとも１段の回路のデジタル－アナログ変換器は、基準電圧を発生する基準電圧発生回路と、共通の端子に接続される複数の容量と、基準電圧発生回路と複数の容量との間に接続され、入力されるデジタル信号に応じて基準電圧発生回路により発生された基準電圧を複数の容量にそれぞれ与える複数のスイッチとを含み、切り替え手段は、基準電圧発生回路により発生される基準電圧を可変に設定する可変部を含むものである。

【００７６】この場合、基準電圧発生回路により発生される基準電圧を変更することにより、基準電圧の電圧レンジを変更することができる。それにより、デジタル－アナログ変換器のフルスケールレンジを容易に切り替えることができる。

【００７７】

【発明の実施の形態】（１）第１の実施の形態

図１は本発明の第１の実施の形態におけるパイプライン型アナログ－デジタル変換回路の構成を示すブロック図

である。図１のアナログ－デジタル変換回路は、１０ビット４段パイプライン構成を有する。

【００７８】図１において、アナログ－デジタル変換回路１は、サンプルホールド回路２、１段目～４段目の回路３～６、複数のラッチ回路７および出力回路８から構成されている。

【００７９】１段目（初段）の回路３は、切り替え可能なフルスケールレンジを有するサブＡ／Ｄコンバータ９ａ、Ｄ／Ａコンバータ１０、切り替え可能な利得を有する演算増幅回路１１ａ、減算回路１２および演算増幅回路１３を備える。減算回路１２および演算増幅回路１３が減算増幅回路１４を構成する。２段目および３段目の回路４，５は、サブＡ／Ｄコンバータ９、Ｄ／Ａコンバータ１０、演算増幅回路１１、減算回路１２および演算増幅回路１３を備える。減算回路１２および演算増幅回路１３が減算増幅回路１４を構成する。４段目（最終段）の回路６は、サブＡ／Ｄコンバータ９のみを備える。

【００８０】図１のパイプライン型アナログ－デジタル変換回路１が図２０の従来のアナログ－デジタル変換回路１００と異なるのは、１段目の回路３に切り替え可能なフルスケールレンジを有するサブＡ／Ｄコンバータ９ａおよび切り替え可能な利得を有する演算増幅回路１１ａが用いられる点である。

【００８１】ここでは、１段目の回路３内のサブＡ／Ｄコンバータ９のフルスケールレンジは、アナログ入力信号の電圧レンジが$V_{IN_{-}-}$のときに、それと等しい電圧レンジ$V_{IN_{-}-}$に切り替えられ、アナログ入力信号の電圧レンジが$V_{IN_{-}-}$／２のときには、それと等しい電圧レンジ$V_{IN_{-}-}$／２に切り替えられる。また、１段目の回路３内の演算増幅回路１１ａの利得は、アナログ入力信号の電圧レンジが$V_{IN_{-}-}$のときには１倍に切り替えられ、アナログ入力信号の電圧レンジが$V_{IN_{-}-}$／２のときには２倍に切り替えられる。

【００８２】１段目～３段目の回路３～５内のＤ／Ａコンバータ１０のフルスケールレンジは固定され、２段目～４段目の回路４～６内のサブＡ／Ｄコンバータ９のフルスケールレンジは固定されている。また、１段目の回路３内の演算増幅回路１３および２段目および３段目の回路３，４内の演算増幅回路１１，１３の利得は２である。

【００８３】１段目の回路３は４ビット構成、２～４段目の回路４～６はそれぞれ２ビット構成である。１～３段目の回路３～５において、サブＡ／Ｄコンバータ９，９ａおよびＤ／Ａコンバータ１０のビット数（ビット構成）は同じに設定されている。

【００８４】アナログ入力信号の電圧レンジが$V_{IN_{-}-}$の場合における図１のアナログ－デジタル変換回路１の動作および各部の電圧レンジは、図２０のアナログ－デジタル変換回路１００と同様である。

【００８５】ここでは、アナログ入力信号の電圧レンジがVIN_{0-0}／２の場合における図１のアナログ－デジタル変換回路１の動作および各部の出力電圧レンジについて説明する。

【００８６】サンプルホールド回路２は、アナログ入力信号Ｖｉｎをサンプリングして一定時間保持する。サンプルホールド回路２から出力されたアナログ入力信号Ｖｉｎは、１段目の回路３へ転送される。

【００８７】１段目の回路３において、サブＡ／Ｄコンバータ９ａは電圧レンジVIN_{0-0}／２のアナログ入力信号Ｖｉｎに対してアナログ－デジタル変換を行う。このときのサブＡ／Ｄコンバータ９ａのフルスケールレンジは、上記のようにVIN_{0-0}／２に切り替えられている。

（１段目の分解能－１）×（Ｄ／Ａコンバータ１０のフルスケールレンジ）／（１段目の分解能）
＝（2^4-1）×（VIN_{0-0}）／2^4
＝１５VIN_{0-0}／１６

一方、演算増幅回路１１ａは、アナログ入力信号Ｖｉｎをサンプリングして増幅および保持する。上記のように、アナログ入力信号の電圧レンジがVIN_{0-0}／２の場合には利得は２倍に切り替えられるので、演算増幅回路１１ａの出力電圧レンジは次式のように表される。

【００９１】
（アナログ入力信号Ｖｉｎの電圧レンジ）×（演算増幅回路１１ａの利得）
＝（VIN_{0-0}／２）×２
＝VIN_{0-0}

減算増幅回路１４は、演算増幅回路１１ａから出力されたアナログ入力信号ＶｉｎとＤ／Ａコンバータ１０のＤ／Ａ変換結果とを減算して増幅する。減算増幅回路１４の出力は、次式のように表される。

【００９２】１段目の減算増幅回路１４の出力電圧レンジは、次式のように表される。

（（演算増幅回路１１ａの出力電圧レンジ）－（Ｄ／Ａコンバータ１０の正規出力電圧レンジ））×（減算増幅回路１４の利得）
＝（（VIN_{0-0}）－（１５VIN_{0-0}／１６））×２
＝VIN_{0-0}／８

２段目の回路４においては、サブＡ／Ｄコンバータ９が、１段目の回路３の減算増幅回路１４の出力に対してＡ／Ｄ変換を行う。サブＡ／Ｄコンバータ９のＡ／Ｄ変換結果は、Ｄ／Ａコンバータ１０へ転送されるとともに、３つのラッチ回路７を介して出力回路８へ転送される。これにより、２段目の回路４から中上位２ビットのデジタル出力（2^3，2^2）が得られる。

【００９３】一方、演算増幅回路１１は、１段目の回路３の減算増幅回路１４の出力を増幅する。減算増幅回路１４は、演算増幅回路１１の出力とＤ／Ａコンバータ１０のＤ／Ａ変換結果とを減算して増幅する。減算増幅回路１４の出力は、３段目の回路５へ転送される。

【００９４】３段目の回路５においては、２段目の回路４の減算増幅回路１４の出力に対して２段目の回路４と同様の動作が行われる。それにより、３段目の回路５から中下位２ビットのデジタル出力（2^1，2^0）が得られる。

【００９５】４段目の回路６においては、３段目の回路５の減算増幅回路１４の出力に対してサブＡ／Ｄコンバータ９がＡ／Ｄ変換を行い、下位２ビットのデジタル出力（2^1，2^0）が得られる。

【００９６】１段目～４段目の回路３～６のデジタル出力は、各ラッチ回路７を経て同時に出力回路８に到達する。すなわち、各ラッチ回路７は各回路３～６のデジタル出力の同期をとるために設けられている。

【００９７】出力回路８は、アナログ入力信号Ｖｉｎの１０ビットのデジタル出力Ｄｏｕｔを必要な場合はデジタル補正処理後パラレル出力する。

【００９８】上記のように、アナログ入力信号の電圧レンジがVIN_{0-0}／２の場合には、１段目の回路３の演算増幅回路１１ａの利得および１段目の回路３のサブＡ／Ｄコンバータ９ａのフルスケールレンジを切り替えることにより、１段目の回路３の減算増幅回路１４から２段目の回路５へ与えられる出力信号の電圧レンジは、アナログ入力信号の電圧レンジがVIN_{0-0}の場合と同様に、VIN_{0-0}／８となる。それにより、アナログ入力信号Ｖｉｎの電圧レンジが半分になったにもかかわらず、アナログ入力信号の電圧レンジは半分になる前と同じデジタル出力が得られる。

【００９９】したがって、回路設計の変更を行うことな

く．アナログ入力信号の電圧レンジの変更に対応したアナログーデジタル変換回路を提供することができる。

【０１００】本実施の形態によれば．回路構成を変更することなく、差動ダブルエンド入力方式のアナログーデジタル変換回路をシングルエンド入力方式のアナログーデジタル変換回路に変更することができる。

【０１０１】図２（ａ）．（ｂ）は図１のアナログーデジタル変換回路１をそれぞれ差動ダブルエンド入力方式およびシングルエンド入力方式に切り替える場合の設定を示す図である。

【０１０２】図２（ａ）に示すように．差動ダブルエンド入力時には．演算増幅回路１１ａの利得を１倍に切り替え．サブＡ／Ｄコンバータ９ａのフルスケールレンジを２ＶｉＮ$_{0-0}$に切り替える。本例では、差動ダブルエンド入力のアナログ入力信号Ｖｉｎの正側アナログ入力電圧Ｖｉｎ（＋）は１．０Ｖから２．０Ｖの範囲で変化し．負側アナログ入力電圧Ｖｉｎ（－）は２．０Ｖから１．０Ｖの範囲で変化する。アナログ入力信号Ｖｉｎの電圧レンジは．次式のようになる。

【０１０３】２ＶｉＮ$_{0-0}$＝｛Ｖｉｎ（＋）－Ｖｉｎ（－）｝の最大値－｛Ｖｉｎ（＋）－Ｖｉｎ（－）｝の最小値＝２．０［Ｖ］

この場合、サブＡ／Ｄコンバータ９ａの正側基準電圧Ｖｒｅｆ（＋）は１．０Ｖから２．０Ｖの範囲で変化し、負側基準電圧Ｖｒｅｆ（－）は２．０Ｖから１．０Ｖの範囲で変化する。

【０１０４】図２（ｂ）に示すように．シングルエンド入力時には、演算増幅回路１１ａの利得を２倍に切り替え．サブＡ／Ｄコンバータ９ａのフルスケールレンジをＶＩＮ$_{0-0}$に切り替える。本例では．シングルエンド入力のアナログ入力信号Ｖｉｎの正側アナログ入力電圧Ｖｉｎ（＋）は１．０Ｖから２．０Ｖの範囲で変化し、負側アナログ入力電圧Ｖｉｎ（－）は１．５Ｖで一定である。アナログ入力信号Ｖｉｎの電圧レンジは、次式のようになる。

【０１０５】ＶＩＮ$_{0-0}$＝｛Ｖｉｎ（＋）－Ｖｉｎ（－）｝の最大値－｛Ｖｉｎ（＋）－Ｖｉｎ（－）｝の最小値＝１．０［Ｖ］

この場合、サブＡ／Ｄコンバータ９ａの正側基準電圧Ｖｒｅｆ（＋）は１．０Ｖから２．０Ｖの範囲で変化し、負側基準電圧Ｖｒｅｆ（－）は１．５Ｖで一定である。

【０１０６】このように．図１のアナログーデジタル変換回路１においては、差動ダブルエンド入力方式をシングルエンド入力方式に変更することによりアナログ入力信号の電圧レンジが１／２になっても．回路構成の再設計が不要となる。

【０１０７】また、シングルエンド入力のアナログ入力信号の電圧レンジを１／２に変更する場合、および差動ダブルエンド入力のアナログ入力信号の電圧レンジを１／２に変更する場合にも．回路構成の再設計が不要となる。

【０１０８】このようにして、同一のＬＳＩ（大規模集積回路）において、アナログ入力信号．演算増幅回路の出力．Ｄ／Ａ変換回路の出力および減算増幅回路の出力の電圧レンジをプログラマブルに変更することができる。その結果．開発期間の短縮化を図ることができるとともに、低消費電力化を行うことも可能である。

【０１０９】（２）第２の実施の形態

図３は本発明の第２の実施の形態におけるパイプライン型アナログーデジタル変換回路の構成を示すブロック図である。図３のアナログーデジタル変換回路１も．１０ビット４段パイプライン構成を有する。

【０１１０】図３において．アナログーデジタル変換回路１は、サンプルホールド回路２，１段目～４段目の回路３～６、複数のラッチ回路７および出力回路８から構成されている。

【０１１１】１段目の回路３は４ビット構成、２～４段目の回路４～６はそれぞれ２ビット構成である。１～３段目の回路３～５において．サブＡ／Ｄコンバータ９，９ｂおよびＤ／Ａコンバータ１０，１０ｂのビット数（ビット構成）は同じに設定されている。

【０１１２】１段目（初段）の回路３は、サブＡ／Ｄコンバータ９，Ｄ／Ａコンバータ１０．演算増幅回路１１．減算回路１２および切り替え可能な利得を有する演算増幅回路１３ａを備える。減算回路１２および演算増幅回路１３ａが減算増幅回路１４ａを構成する。

【０１１３】２段目および３段目の回路４，５は．切り替え可能なフルスケールレンジを有するサブＡ／Ｄコンバータ９ｂ、切り替え可能なフルスケールレンジを有するＤ／Ａコンバータ１０ｂ．演算増幅回路１１．減算回路１２および演算増幅回路１３を備える。減算回路１２および演算増幅回路１３が減算増幅回路１４を構成する。４段目（最終段）の回路６は、切り替え可能なフルスケールレンジを有するサブＡ／Ｄコンバータ９ｂのみを備える。

【０１１４】ここでは、２段目～４段目のサブＡ／Ｄコンバータ９ｂが．図２０の２段目～４段目のサブＡ／Ｄコンバータ９の２倍の精度を有するものとする。以下、２段目～４段目に２倍の精度を有するサブＡ／Ｄコンバータ９ｂを用いた場合のアナログーデジタル変換回路１の再設計について説明する。

【０１１５】１段目の回路３内の減算増幅回路１４ａの利得は１倍と２倍とに切り替え可能である。また．２段目～４段目の回路４～６内のサブＡ／Ｄコンバータ９ｂのフルスケールレンジはＶＩＮ$_{0-0}$／８とＶＩＮ$_{0-0}$／１６とに切り替え可能である。さらに．２段目および３段目の回路４．５内のＤ／Ａコンバータ１０ｂのフルスケールレンジはＶＩＮ$_{0-0}$／４とＶＩＮ$_{0-0}$／８とに切り替え可能である。

【０１１６】ここでは、１段目の回路３内の減算増幅回

路１４ａの利得を１倍に切り替える。また、２段目～４段目の回路４～６内のサブA／Dコンバータ９ｂのフルスケールレンジをVIN_{0-0}／１６に切り替え．２段目および３段目の回路４，５内のD／Aコンバータ１０ｂのフルスケールレンジをVIN_{0-0}／８に切り替える。１段目の回路３内のサブA／Dコンバータ９のフルスケールレンジはVIN_{0-0}である。また．２段目および３段目の回路３、４内の演算増幅回路１１，１３の利得は２である。

【０１１７】ここでは、アナログ入力信号の電圧レンジがVIN_{0-0}の場合における図１のアナログ－デジタル変換回路１の動作および各部の出力電圧レンジについて説明する。

【０１１８】サンプルホールド回路２は、アナログ入力信号Ｖｉｎをサンプリングして一定時間保持する。サンプルホールド回路２から出力されたアナログ入力信号Ｖｉｎは、１段目の回路３へ転送される。

一方．演算増幅回路１１は．アナログ入力信号Ｖｉｎをサンプリングして増幅および保持する。演算増幅回路１１の利得は１倍であるので．演算増幅回路１１の出力電

減算増幅回路１４ａは、演算増幅回路１１から出力されたアナログ入力信号ＶｉｎとD／Aコンバータ１０のD／A変換結果とを減算して増幅する。減算増幅回路１４ａの出力は、２段目の回路４へ転送される。

２段目の回路４においては．サブA／Dコンバータ９ｂが．１段目の回路３の減算増幅回路１４ａの出力に対してA／D変換を行う。サブA／Dコンバータ９ｂのA／D変換結果は．D／Aコンバータ１０ｂへ転送されるとともに、３つのラッチ回路７を介して出力回路８へ転送される。

【０１２６】この場合、サブA／Dコンバータ９ｂは、図２０のサブA／Dコンバータ９の２倍の精度を有するので．図２０のサブA／Dコンバータ９の半分のフルスケールレンジVIN_{0-0}／１６で２段目の回路４から中上位２ビットのデジタル出力（2^1，2^0）が得られる。

＊【０１１９】１段目の回路３において．サブA／Dコンバータ９は高圧レンジVIN_{0-0}のアナログ入力信号Ｖｉｎに対してアナログ－デジタル変換を行う。このときのサブA／Dコンバータ９のフルスケールレンジはVIN_{0-0}である。

【０１２０】サブA／Dコンバータ９のA／D変換結果である上位４ビットのデジタル出力（2^3，2^2，2^1，2^0）は．D／Aコンバータ１０へ転送されるとともに、４つのラッチ回路７を介して出力回路８へ転送される。D／Aコンバータ１０は、サブA／Dコンバータ９のA／D変換結果である上位４ビットのデジタル出力をアナログ信号に変換する。

【０１２１】D／Aコンバータ１０のフルスケールレンジは固定されているので．D／Aコンバータ１０の正規出力電圧レンジは、次式のように表される。

【０１２２】

（１段目の分解能－１）×（D／Aコンバータ１０のフルスケールレンジ）／（１段目の分解能）
＝（2^4-1）×（VIN_{0-0}）／2^4
＝１５VIN_{0-0}／１６

※圧レンジは次式のように表される。

【０１２３】

（アナログ入力信号Ｖｉｎの電圧レンジ）×（演算増幅回路１１の利得）
＝VIN_{0-0}×１
＝VIN_{0-0}

★【０１２４】１段目の減算増幅回路１４ａの利得は１に切り替えられているので．１段目の減算増幅回路１４ａの出力電圧レンジは、次式のように表される。

【０１２５】

（（演算増幅回路１１の出力電圧レンジ）－（D／Aコンバータ１０の正規出力電圧レンジ））×（減算増幅回路１４ａの利得）
＝（（VIN_{0-0}）－（１５VIN_{0-0}／１６））×１
＝VIN_{0-0}／１６

☆る。

【０１２７】D／Aコンバータ１０ｂは、サブA／Dコンバータ９ｂのA／D変換結果である中上位２ビットのデジタル出力をアナログ信号に変換する。

【０１２８】D／Aコンバータ１０ｂのフルスケールレンジは図２０のD／Aコンバータ１０の半分のVIN_{0-0}／８に切り替えられているので．D／Aコンバータ１０ｂの正規出力電圧レンジは、次式のように表される。

【０１２９】

（２段目の分解能－１）×（D／Aコンバータ１０ｂのフルスケールレンジ）／（２段目の分解能）
＝（2^4-1）×（VIN_{0-0}／８）／2^2
＝３VIN_{0-0}／３２

$$Vo(-)=(Vin(-)-VRT1)\cdot(CA/CB)$$

$$\triangle Vo=Vo(+)-Vo(-)$$

$$=(Vin(+)-Vin(-))\cdot(CA/CB)$$

したがって、容量値切り替え回路１１１，１１２の容量値ＣＢを切り替えることにより、演算増幅回路１１ａの利得を切り替えることができる。

【０１４３】図５は図１のアナログ－デジタル変換回路１における演算増幅回路１１ａの構成の第２の例を示す回路図である。

【０１４４】図５の演算増幅回路１１ａは、演算増幅器１１０、コンデンサ１２３，１２４，容量値切り替え回路１２５，１２６およびスイッチ１１５～１２２を含む。

【０１４５】演算増幅器１１０の反転入力端子と反転出力端子との間にフィードバック容量としてコンデンサ１２３が接続され，非反転入力端子と非反転出力端子との間にフィードバック容量としてコンデンサ１２４が接続されている。また、演算増幅器１１０の反転入力端子に入力容量として容量値切り替え回路１２５が接続され、非反転入力端子に入力容量として容量値切り替え回路１＊２６が接続されている。

【０１４６】正側アナログ入力電圧Ｖｉｎ（＋）および中間基準電圧ＶＲＴ１がそれぞれスイッチ１１５，１１６を介して容量値切り替え回路１２５に与えられる。また，負側アナログ入力電圧Ｖｉｎ（－）および中間基準電圧ＶＲＴ１がそれぞれスイッチ１１７，１１８を介して容量値切り替え回路１２６に与えられる。演算増幅器１１０の反転入力端子、反転出力端子，非反転入力端子および非反転出力端子は，それぞれスイッチ１１９，１２０，１２１，１２２を介して接地されている。

【０１４７】ここで，容量値切り替え回路１２５，１２６の容量値をそれぞれＣＣとし、コンデンサ１２３，１２４の容量値をそれぞれＣＤとすると，演算増幅器１１０の反転出力端子の正側アナログ出力電圧Ｖｏ（＋）および非反転出力端子の負側アナログ出力電圧Ｖｏ（－）は次式のようになる。

【０１４８】

$$Vo(+)=(Vin(+)-VRT1)\cdot(CC/CD)$$

$$Vo(-)=(Vin(-)-VRT1)\cdot(CC/CD)$$

$$\triangle Vo=Vo(+)-Vo(-)$$

$$=(Vin(+)-Vin(-))\cdot(CC/CD)$$

したがって、容量値切り替え回路１２５，１２６の容量値ＣＣを切り替えることにより、演算増幅回路１１ａの利得を切り替えることができる。

【０１４９】図６～図１１は演算増幅回路１１ａの具体的な回路構成の第１～第６の例を示す回路図である。

【０１５０】図６～図１１において，コンデンサＣａ，Ｃｂ，Ｃｃの各々は等しい容量値Ｃを有するものとする。また、ｍを任意の正の整数とする。

【０１５１】図６の例では，演算増幅器１１０の反転入力端子と反転出力端子との間にｍ個のコンデンサＣａの並列回路とスイッチＳａとが直列に接続され，かつｍ個のコンデンサＣａの並列回路が接続されている。ここで，ｍは任意の正の整数である。同様に、演算増幅器１１０の非反転入力端子と非反転出力端子との間にｍ個のコンデンサＣａの並列回路とスイッチＳａとが直列に接続され，かつｍ個のコンデンサＣａの並列回路が接続されている。また，演算増幅器１１０の反転入力端子に２ｍ個のコンデンサＣｂが接続され、非反転入力端子に２ｍ個のコンデンサＣｂが接続されている。

【０１５２】正側アナログ入力電圧Ｖｉｎ（＋）がそれぞれスイッチＳ１を介して反転入力端子側の２ｍ個のコンデンサＣｂに与えられる。また、負側アナログ入力電圧Ｖｉｎ（－）がそれぞれスイッチＳ１を介して非反転入力端子側のコンデンサＣｂに与えられる。高電位側基準電圧ＶＲＴがそれぞれスイッチＳ２を介して反転入力端子側のｍ個のコンデンサＣｂおよび非反転入力端子側のｍ個のコンデンサＣｂに与えられ，低電位側基準電圧ＶＲＢがそれぞれスイッチＳ２を介して非反転入力端子側のｍ個のコンデンサＣｂおよび非反転入力端子側のｍ個のコンデンサＣｂに与えられる。

【０１５３】本例では，入力容量の値は２ｍＣである。スイッチＳａをオンにすると、フィードバック容量の値が２ｍＣとなり，スイッチＳａをオフにすると，フィードバック容量の値がｍＣとなる。したがって，差動ダブルエンド入力時には，スイッチＳａをオンに切り替えることにより利得が１倍となり、シングルエンド入力時には，スイッチＳａをオフに切り替えることにより利得が２倍となる。

【０１５４】図７の例では，演算増幅器１１０の反転入力端子と反転出力端子との間に２ｍ個のコンデンサＣａの並列回路と２ｍ個のコンデンサＣｃの並列回路とが直列に接続され，かつコンデンサＣｃに並列にスイッチＳａが接続されている。同様に、演算増幅器１１０の非反転入力端子と非反転出力端子との間に２ｍ個のコンデンサＣａの並列回路と２ｍ個のコンデンサＣｃの並列回路とが直列に接続され，かつコンデンサＣｃに並列にスイッチＳａが接続されている。図７の演算増幅回路１１ａの他の部分の構成は、図６の演算増幅回路１１ａと同様である。

【０１５５】本例では，入力容量の値は２ｍＣである。スイッチＳａをオンにすると、フィードバック容量の値が２ｍＣとなり，スイッチＳａをオフにすると，フィー

ドバック容量の値がｍＣとなる。したがって、差動ダブルエンド入力時には、スイッチＳａをオンに切り替えることにより利得が１倍となり、シングルエンド入力時には、スイッチＳａをオフに切り替えることにより利得が２倍となる。

【０１５６】図８の例では、演算増幅器１１０の反転入力端子と反転出力端子との間に２ｍ個のコンデンサＣａの並列回路と２ｍ個のコンデンサＣｃの並列回路とが直列に接続され、かつコンデンサＣａに並列にスイッチＳａが接続されている。同様に、演算増幅器１１０の非反転入力端子と非反転出力端子との間に２ｍ個のコンデンサＣａの並列回路と２ｍ個のコンデンサＣｃの並列回路とが直列に接続され、かつコンデンサＣａに並列にスイッチＳａが接続されている。図８の演算増幅回路１１ａの他の部分の構成は、図６の演算増幅回路１１ａと同様である。

【０１５７】本例では、入力容量の値は２ｍＣである。スイッチＳａをオンにすると、フィードバック容量の値が２ｍＣとなり、スイッチＳａをオフにすると、フィードバック容量の値がｍＣとなる。したがって、差動ダブルエンド入力時には、スイッチＳａをオンに切り替えることにより利得が１倍となり、シングルエンド入力時には、スイッチＳａをオフに切り替えることにより利得が２倍となる。

【０１５８】図９の例では、演算増幅器１１０の反転入力端子と反転出力端子との間にｍ個のコンデンサＣａの並列回路が接続されている。同様に、演算増幅器１１０の非反転入力端子と非反転出力端子との間にｍ個のコンデンサＣａの並列回路が接続されている。また、演算増幅器１１０の反転入力端子に２ｍ個のコンデンサＣｂが接続され、非反転入力端子に２ｍ個のコンデンサＣｂが接続されている。

【０１５９】正側アナログ入力電圧Ｖｉｎ（＋）がそれぞれスイッチＳ１，Ｓ１ａを介して反転入力端子側の２ｍ個のコンデンサＣｂに与えられる。また、負側アナログ入力電圧Ｖｉｎ（－）がそれぞれスイッチＳ１，Ｓ１ａを介して非反転入力端子側のコンデンサＣｂに与えられる。高電位側基準電圧ＶＲＴがそれぞれスイッチＳ２，Ｓ２ａを介して反転入力端子側のｍ個のコンデンサＣｂおよび非反転入力端子側のｍ個のコンデンサＣｂに与えられ、低電位側基準電圧ＶＲＢがそれぞれスイッチＳ２，Ｓ２ａを介して非反転入力端子側のｍ個のコンデンサＣｂおよび非反転入力端子側のｍ個のコンデンサＣｂに与えられる。

【０１６０】本例では、フィードバック容量の値はｍＣである。スイッチＳ１ａ，Ｓ２ａをオンにすると、入力容量の値が２ｍＣとなり、スイッチＳ１ａ，Ｓ２ａをオフにすると、入力容量の値がｍＣとなる。したがって、差動ダブルエンド入力時には、スイッチＳ１ａ，Ｓ２ａを常にオフにすることにより利得が１倍となり、シングルエンド入力時には、スイッチＳ１ａ，Ｓ２ａをスイッチＳ１，Ｓ２と同様にスイッチング動作することにより利得が２倍となる。

【０１６１】図１０の例では、演算増幅器１１０の反転入力端子と反転出力端子との間にｍ個のコンデンサＣａの並列回路が接続されている。同様に、演算増幅器１１０の非反転入力端子と非反転出力端子との間にｍ個のコンデンサＣａの並列回路が接続されている。また、演算増幅器１１０の反転入力端子に２ｍ個のコンデンサＣｃの並列回路が接続され、コンデンサＣｃの並列回路に２ｍ個のコンデンサＣｂが接続され、コンデンサＣｃに並列にスイッチＳａが接続されている。また、非反転入力端子に２ｍ個のコンデンサＣｃの並列回路が接続され、コンデンサＣｃの並列回路に２ｍ個のコンデンサＣｂが接続され、コンデンサＣｃに並列にスイッチＳａが接続されている。図１０の演算増幅回路１１ａの他の部分の構成は、図６の演算増幅回路１１ａと同様である。

【０１６２】本例では、フィードバック容量の値はｍＣである。スイッチＳａをオンにすると、入力容量の値が２ｍＣとなり、スイッチＳａをオフにすると、入力容量の値がｍＣとなる。したがって、差動ダブルエンド入力時には、スイッチＳａをオフにすることにより利得が１倍となり、シングルエンド入力時には、スイッチＳａをオンにすることにより利得が２倍となる。

【０１６３】図１１の例では、演算増幅器１１０の反転入力端子と反転出力端子との間にｍ個のコンデンサＣａの並列回路が接続されている。同様に、演算増幅器１１０の非反転入力端子と非反転出力端子との間にｍ個のコンデンサＣａの並列回路が接続されている。また、演算増幅器１１０の反転入力端子に２ｍ個のコンデンサＣｃの並列回路が接続され、コンデンサＣｃの並列回路に２ｍ個のコンデンサＣｂが接続され、コンデンサＣｂに並列にスイッチＳａが接続されている。また、非反転入力端子に２ｍ個のコンデンサＣｃの並列回路が接続され、コンデンサＣｃの並列回路に２ｍ個のコンデンサＣｂが接続され、コンデンサＣｂに並列にスイッチＳａが接続されている。図１１の演算増幅回路１１ａの他の部分の構成は、図６の演算増幅回路１１ａの構成と同様である。

【０１６４】本例では、フィードバック容量の値はｍＣである。スイッチＳａをオンにすると、入力容量の値が２ｍＣとなり、スイッチＳａをオフにすると、入力容量の値がｍＣとなる。したがって、差動ダブルエンド入力時には、スイッチＳａをオフにすることにより利得が１倍となり、シングルエンド入力時には、スイッチＳａをオンにすることにより利得が２倍となる。

【０１６５】図６～図１１の演算増幅回路１１ａにおいて、上記のように、スイッチＳａはＭＯＳトランジスタにより構成される。それにより、スイッチＳａが接続されるノードにはＭＯＳトランジスタの拡散容量が付加さ

れ．スイッチＳａのオン時にはゲート容量が付加される。演算増幅器１１０の反転入力端子または非反転入力端子に容量が付加されると．演算増幅回路１１ａの動作速度が低下する。

【０１６６】図６および図７の例では．スイッチＳａが演算増幅器１１０の反転出力端子および非反転出力端子に接続されている。それにより．演算増幅回路１１ａの動作速度が低下しない。したがって．図６および図７の例が好ましい。

【０１６７】また、スイッチＳａがコンデンサに並列に接続された場合．スイッチＳａのオン時にオン抵抗が存在するため、コンデンサの容量を完全に切り離すことができない。

【０１６８】図６の例では．スイッチＳａがコンデンサＣａに直列に接続されかつスイッチＳａが演算増幅器１１０の反転出力端子および非反転出力端子に接続されている。それにより、スイッチＳａのオン時に、コンデンサＣａの容量を完全に切り離すことができる。したがって．図６の例が最も好ましい。

【０１６９】また、図９の例では、スイッチＳ１ａ，Ｓ２ａがコンデンサＣｂよりも入力側に接続されている。逆に．コンデンサＣｂがスイッチＳ１ａ，Ｓ２ａよりも入力側に接続されている場合、スイッチＳ１ａ、Ｓ２ａがオフ状態に設定されても．コンデンサＣｂの寄生容量が充電される。それにより．利得の設定時に、寄生容量を考慮する必要が生じ、寄生容量のばらつきにより利得がばらつくことになる。図９の例のように、スイッチＳ１ａ．Ｓ２ａがコンデンサＣｂよりも入力側に接続されることにより．スイッチＳ１ａ，Ｓ２ａがオフ状態に設定された場合にスイッチＳ１ａ，Ｓ２ａによりコンデンサＣｂが寄生容量とともに切り離される。したがって、図９の例では．利得の設定時にコンデンサＣｂの寄生容量を考慮する必要がなくなり、寄生容量のばらつきによる利得のばらつきがなくなる。

【０１７０】図１２は図１のアナログ－デジタル変換回路１におけるサブＡ／Ｄコンバータ９ａの構成の第１の例を示す回路図．図１３は図１２のサブＡ／Ｄコンバータ９ａに用いられるコンパレータの構成を示す回路図である。

【０１７１】図１２において、サブＡ／Ｄコンバータ９ａは．基準電圧を発生する基準電圧発生回路９２．９３ａ．９３ｂおよび複数のコンパレータ９０を備える。

【０１７２】基準電圧発生回路９２は．直列に接続された複数の抵抗Ｒからなる。基準電圧発生回路９３ａは、直列に接続された複数の抵抗Ｒからなる。基準電圧発生回路９３ｂは．直列に接続された複数の抵抗Ｒ１からなる。複数の抵抗Ｒは等しい抵抗値を有し、複数の抵抗Ｒ１は等しい抵抗値を有する。

【０１７３】基準電圧発生回路９２は．高電位側基準電圧ＶＲＴを受けるノードＮ９１と低電位側基準電圧ＶＲＢを受けるノードＮ９２との間に接続されている。基準電圧発生回路９３ａは、高電位側基準電圧ＶＲＴを受けるノードＮ９３と低電位側基準電圧ＶＲＢを受けるノードＮ９４との間に、スイッチＳ２４．Ｓ２５を介して接続されている。基準電圧発生回路９３ｂは、高電位側基準電圧ＶＲＴを受けるノードＮ９３と低電位側基準電圧ＶＲＢを受けるノードＮ９４との間に接続されている。基準電圧発生回路９３ａの中間ノードＮ９５と基準電圧発生回路９３ｂの中間ノードＮ９６との間には．スイッチＳ２６が接続されている。

【０１７４】基準電圧発生回路９２の抵抗Ｒ間の接続点にそれぞれ異なる基準電圧が生成される。同様に．基準電圧発生回路９３ａの抵抗Ｒ間の接続点にそれぞれ異なる基準電圧が生成される。ここでは．基準電圧発生回路９２により得られる異なる基準電圧を正側基準電圧Ｖｒｅｆ（＋）と呼ぶ。基準電圧発生回路９３ａにより得られる異なる基準電圧を負側基準電圧Ｖｒｅｆ（－）と呼ぶ。

【０１７５】基準電圧発生回路９３ｂの中間ノードＮ９６には、高電位側基準電圧ＶＲＴと低電位側基準電圧ＶＲＢとの中間の電圧である中間基準電圧ＶＲＴ１（＝（ＶＲＴ－ＶＲＢ）／２）が生成される。

【０１７６】図１３に示すように、各コンパレータ９０は．演算増幅器９１、コンデンサＣ１．Ｃ２およびスイッチＳ１３～Ｓ１８を含む。演算増幅器９１の反転入力端子と反転出力端子との間にスイッチＳ１３が接続され．非反転入力端子と非反転出力端子との間にスイッチＳ１４が接続されている。また、演算増幅器９１の反転入力端子にはコンデンサＣ１が接続され、非反転入力端子にはコンデンサＣ２が接続されている。コンデンサＣ１にはスイッチＳ１５，Ｓ１６が接続され、コンデンサＣ２にはスイッチＳ１７．Ｓ１８が接続されている。なお．図１２では．各コンパレータ９０のスイッチＳ１３、Ｓ１４の図示を省略している。

【０１７７】正側アナログ入力電圧Ｖｉｎ（＋）および正側基準電圧Ｖｒｅｆ（＋）がそれぞれスイッチＳ１５．Ｓ１６を介してコンデンサＣ１に与えられる。また．負側アナログ入力電圧Ｖｉｎ（－）および負側基準電圧Ｖｒｅｆ（－）がそれぞれスイッチＳ１７．Ｓ１８を介してコンデンサＣ２に与えられる。

【０１７８】初期状態では．スイッチＳ１３，Ｓ１４，Ｓ１５，Ｓ１７がオンし．スイッチＳ１６，Ｓ１８がオフしている。次に、スイッチＳ１３．Ｓ１４をオフした後．スイッチＳ１５，Ｓ１７をオフし．スイッチＳ１６．Ｓ１８をオンする。スイッチＳ１３，Ｓ１４をオフした時点で、演算増幅器９１の反転入力端子および非反転入力端子がフローティング状態となっているので、反転入力端子の電圧が（Ｖｉｎ（＋）－Ｖｒｅｆ（＋））遷移し、非反転入力端子の電圧が（Ｖｉｎ（－）－Ｖｒｅｆ（－））遷移する。結果的に、差動アナログ入力電

圧（Ｖｉｎ（＋）－Ｖｉｎ（－））と差動基準電圧（Ｖｒｅｆ（＋）－Ｖｒｅｆ（－））とが比較され．比較結果に応じて正側アナログ出力電圧Ｖｏｕｔ（＋）および負側アナログ出力電圧Ｖｏｕｔ（－）が変化する。

【０１７９】図１２の複数のコンパレータ９０の比較結果をエンコーダ９５０によってエンコードすることにより．デジタルコードＤｃｏｄｅを得ることができる。

【０１８０】図１２のサブＡ／Ｄコンバータ９ａにおいて．差動ダブルエンド入力時には、スイッチＳ２４，Ｓ２５をオンし．スイッチＳ２６をオフする。それにより．各コンパレータ９０のコンデンサＣ２にスイッチＳ１８を介して基準電圧発生回路９３ａによりそれぞれ異なる負側基準電圧Ｖｒｅｆ（－）が与えられる。シングルエンド入力時には、スイッチＳ２４．Ｓ２５をオフし．スイッチＳ２６をオンにする。それにより．各コンパレータ９０のコンデンサＣ２にスイッチＳ１８を介して基準電圧発生回路９３ｂにより中間基準電圧ＶＲＴ１が与えられる。

【０１８１】このようにして、サブＡ／Ｄコンバータ９ａにおいて、フルスケールレンジが切り替えられる。

【０１８２】なお、基準電圧発生回路９３ｂを設けずに．スイッチＳ２６を基準電圧発生回路９３ａの中間ノードＮ９５と基準電圧発生回路９２の中間ノードとの間に接続してもよい。

【０１８３】図１４は図１のアナログ－デジタル変換回路１におけるサブＡ／Ｄコンバータ９ａの構成の第２の例を示す回路図．図１５は図１４のサブＡ／Ｄコンバータ９ａに用いられるコンパレータの構成を示す回路図である。

【０１８４】図１４において、基準電圧発生回路９３ａの中間ノードＮ９５と基準電圧発生回路９３ｂの中間ノードＮ９６との間には、図１２のスイッチＳ２６が接続されていない。

【０１８５】図１５に示すように、各コンパレータ９０は．演算増幅器９１、コンデンサＣ１．Ｃ２およびスイッチＳ１３～Ｓ１８を含み．さらにスイッチＳ２１，Ｓ２２を含む。スイッチＳ２１の一端はコンデンサＣ１に接続され、スイッチＳ２１の他端は開放されている。スイッチＳ２２の一端はコンデンサＣ２に接続され．他端は図１４の基準電圧発生回９３ｂの中間ノードＮ９６に接続されている。図１５のコンパレータ９０の他の部分の構成は、図１３のコンパレータ９０の構成と同様である。

【０１８６】基準電圧発生回９３ｂにより中間基準電圧ＶＲＴ１がスイッチＳ２２を介してコンデンサＣ２に与えられる。

【０１８７】差動ダブルエンド入力時の図１５のコンパレータ９０の動作は、図１３のコンパレータ９０の動作と同様である。このとき．スイッチＳ２１，Ｓ２２は常時オフしている。シングルエンド入力時には、スイッチＳ１８の代わりにスイッチＳ２２を動作させる。このとき．スイッチＳ２１は常時オフしている。

【０１８８】図１４のサブＡ／Ｄコンバータ９ａにおいて．差動ダブルエンド入力時には、スイッチＳ２４，Ｓ２５をオンする。このとき．スイッチＳ２１，Ｓ２２は常時オフにする。それにより、各コンパレータ９０のコンデンサＣ２にスイッチＳ１８を介して基準電圧発生回路９３ａによりそれぞれ異なる負側基準電圧Ｖｒｅｆ（－）が与えられる。シングルエンド入力時には、スイッチＳ２４，Ｓ２５をオフし、スイッチＳ１８の代わりにスイッチＳ２２を動作させる。このとき、スイッチＳ２１は常時オフしている。それにより．各コンパレータ９０のコンデンサＣ２にスイッチＳ２２を介して基準電圧発生回路９３ｂにより中間基準電圧ＶＲＴ１が与えられる。

【０１８９】このようにして、サブＡ／Ｄコンバータ９ａにおいて、フルスケールレンジが切り替えられる。

【０１９０】なお、各コンパレータ９０にスイッチＳ２１を設けなくてもよいが．コンパレータ９０の回路構成の対称性を確保するためには、スイッチＳ２１を設けることが好ましい。

【０１９１】図１６は図３のアナログ－デジタル変換回路１における２段目の回路４内のサブＡ／Ｄコンバータ９ｂの回路図である。図１６のサブＡ／Ｄコンバータ９ｂは全並列比較（フラッシュ）方式サブＡ／Ｄコンバータである。

【０１９２】サブＡ／Ｄコンバータ９ｂは、基準電圧を発生する基準電圧発生回路９４，９５および複数個のコンパレータ９０から構成される。基準電圧発生回路９４．９５の各々は、抵抗Ｒ２、２ｎ個の抵抗Ｒおよび抵抗Ｒ３からなる。抵抗Ｒ２、Ｒ３はそれぞれ抵抗Ｒのｎ倍の抵抗値を有する。抵抗Ｒ２、２ｎ個の抵抗Ｒおよび抵抗Ｒ３は、高電位側基準電圧ＶＲＴ２を受けるノードＮ９７と低電位側基準電圧ＶＲＢ２を受けるノードＮ９８との間に接続されている。抵抗Ｒ２の両端にはスイッチＳ２８が接続され．抵抗Ｒ３の両端にはスイッチＳ２９が接続されている。

【０１９３】基準電圧発生回路９４の抵抗Ｒ間の接続点にそれぞれ異なる基準電圧が生成される。同様に．基準電圧発生回路９５の抵抗Ｒ間の接続点にそれぞれ異なる基準電圧が生成される。ここでは、基準電圧発生回路９４により得られる異なる基準電圧を正側基準電圧Ｖｒｅｆ（＋）と呼ぶ。基準電圧発生回路９５により得られる異なる基準電圧を負側基準電圧Ｖｒｅｆ（－）と呼ぶ。

【０１９４】正側アナログ入力電圧Ｖｉｎ（＋）および正側基準電圧Ｖｒｅｆ（＋）がそれぞれスイッチＳ１５．Ｓ１６を介して各コンパレータ９０のコンデンサＣ１に与えられる。また、負側アナログ入力電圧Ｖｉｎ（－）および負側基準電圧Ｖｒｅｆ（－）がそれぞれスイッチＳ１７．Ｓ１８を介して各コンパレータ９０のコ

ンデンサＣ２に与えられる。図１６のコンパレータ９０の構成および動作は、図１３のコンパレータ９０の構成および動作と同様である。

【０１９５】ここで、高電位側基準電圧ＶＲＴ２と低電位側基準電圧ＶＲＢ２との差はＶｉＮ。。。／８に設定される。基準電圧発生回路９５，９６のスイッチＳ２８，Ｓ２９がオフの場合には、フルスケールレンジはＶｉＮ。。。／１６である。また、スイッチＳ２８，Ｓ２９をオンにすると、フルスケールレンジはＶＩＮ。。。／８となる。このようにして、サブＡ／Ｄコンバータ９ｂでは、フルスケールレンジを１倍と２倍とに切り替えることができる。

【０１９６】図１７は図３のアナログ－デジタル変換回路１における２段目の回路４内のＤ／Ａコンバータ１０の回路図である。図１７のＤ／Ａコンバータ１０は容量アレイ方式Ｄ／Ａコンバータである。

【０１９７】Ｄ／Ａコンバータ１０は、基準電圧を発生する基準電圧発生回路９６、アレイ状に接続されたそれぞれ複数個の正側のスイッチＳ５１、Ｓ５２、複数個の負側のスイッチＳ５３，Ｓ５４、複数個の正側コンデンサＣ５０、および複数個の負側コンデンサＣ５１から構成される。

【０１９８】基準電圧発生回路９６は、抵抗Ｒ４、複数個の抵抗Ｒおよび抵抗Ｒ５からなる。抵抗Ｒ４、Ｒ５は、複数個の抵抗Ｒの合計の抵抗値の半分の抵抗値を有する。抵抗Ｒ４、複数個の抵抗Ｒおよび抵抗Ｒ５は、高電位側基準電圧ＶＲＴ３を受けるノードＮ１０１と低電位側基準電圧ＶＲＢ３を受けるノードＮ１０２との間に直列に接続されている。抵抗Ｒ４の両端にはスイッチＳ３０が接続され、抵抗Ｒ５の両端にはスイッチＳ３１が接続されている。

【０１９９】コンデンサＣ５０，Ｃ５１はすべて同じ容量値を有する。コンデンサＣ５０の一方の端子（以下、出力端子と呼ぶ）Ｎ１１１からは差動正側出力電圧ＶＤＡ（＋）が生成され、コンデンサＣ５１の一方の端子（以下、出力端子という）Ｎ１１２からは差動負側出力電圧ＶＤＡ（－）が生成される。なお、各コンデンサＣ５０、Ｃ５１の他方の端子を入力端子と呼ぶ。

【０２００】各スイッチＳ５１の一方の端子は抵抗Ｒ４と抵抗Ｒとの間のノードＮ１０３に接続され、他方の端子はコンデンサＣ５０の入力端子に接続されている。各スイッチＳ５２の一方の端子は抵抗Ｒ５と抵抗Ｒとの間のノードＮ１０４に接続され、他方の端子はコンデンサＣ５０の入力端子に接続されている。各スイッチＳ５３の一方の端子は抵抗Ｒ４と抵抗Ｒとの間のノードＮ１０３に接続され、他方の端子はコンデンサＣ５１の入力端子に接続されている。各スイッチＳ５４の一方の端子は抵抗Ｒ５と抵抗Ｒとの間のノードＮ１０４に接続され、他方の端子はコンデンサＣ５１の入力端子に接続されている。

【０２０１】スイッチＳ５１，Ｓ５２、Ｓ５３、Ｓ５４は、図１６のサブＡ／Ｄコンバータ９ｂのコンパレータ９０の出力レベルに従ってオンオフ動作する。同じコンパレータ９０の出力信号を受ける４個のスイッチＳ５１、Ｓ５２，Ｓ５３，Ｓ５４が４連スイッチを構成する。例えば、１つのコンパレータ９０の出力がハイレベルの場合、４連スイッチのスイッチＳ５１，Ｓ５４がオンし、スイッチＳ５２，Ｓ５３がオフする。逆に、１つのコンパレータ９０の出力がローレベルの場合、４連スイッチのスイッチＳ５１、Ｓ５４がオフし、スイッチＳ５２、Ｓ５３がオンする。

【０２０２】サブＡ／Ｄコンバータ９ｂの複数のコンパレータ９０の出力レベルに応じて複数のスイッチＳ５１、Ｓ５２，Ｓ５３，Ｓ５４がオンオフ動作し、出力端子Ｎ１１１，Ｎ１１２に差動正側出力電圧ＶＤＡ（＋）および差動負側出力電圧ＶＤＡ（－）が得られる。

【０２０３】ここで、高電位側基準電圧ＶＲＴ３と低電位側基準電圧ＶＲＢ３との差はＶｉＮ。。。／４に設定される。基準電圧発生回路９６のスイッチＳ３０、Ｓ３１がオフの場合には、フルスケールレンジはＶｉＮ。。。／８である。スイッチＳ３０、Ｓ３１をオンにすると、フルスケールレンジはＶｉＮ。。。／４となる。このようにして、Ｄ／Ａコンバータ１０ｂでは、フルスケールレンジを１倍と２倍とに切り替えることができる。

【０２０４】図１８は図３のアナログ－デジタル変換回路１における演算増幅回路１４ａの構成の第１の例を示す回路図である。

【０２０５】図１８の演算増幅回路１４ａは、演算増幅器１３０、容量値切り替え回路１３１、１３２、コンデンサ１３３，１３４およびスイッチ１３５～１３８を含む。スイッチは、例えばＭＯＳ（金属酸化物半導体）トランジスタにより構成される。

【０２０６】演算増幅器１３０の反転入力端子と反転出力端子との間にフィードバック容量として容量値切り替え回路１３１が接続され、非反転入力端子と非反転出力端子との間にフィードバック容量として容量値切り替え回路１３２が接続されている。また、演算増幅器１３０の反転入力端子に入力容量としてコンデンサ１３３が接続され、非反転入力端子に入力容量としてコンデンサ１３４が接続されている。

【０２０７】図３の演算増幅回路１１から出力される正側アナログ出力電圧Ｖｏ（＋）およびＤ／Ａコンバータ１０ｂから出力される差動正側出力電圧ＶＤＡ（＋）がそれぞれスイッチ１３５、１３６を介してコンデンサ１３３に与えられる。また、演算増幅回路１１から出力される負側アナログ出力電圧Ｖｏ（－）およびＤ／Ａコンバータ１０ｂから出力される差動正側出力電圧ＶＤＡ（－）がそれぞれスイッチ１３７，１３８を介してコンデンサ１３４に与えられる。演算増幅器１３０の反転入力端子、反転出力端子、非反転入力端子および非反転出

力端子は、それぞれスイッチ１３９、１４０、１４１、１４２を介して接地されている。

【０２０８】図１８の減算増幅回路１４ａの動作は、図４の演算増幅回路１１ａの動作と同様である。演算増幅器１３０の反転出力端子および非反転出力端子からは次段の回路４へ与えられる正側アナログ入力電圧Ｖｉｎ（＋）および負側アナログ入力電圧Ｖｉｎ（－）が得られる。

【０２０９】ここで、容量値切り替え回路１３１、１３２の容量値を切り替えることにより、減算増幅回路１４ａの利得を切り替えることができる。

【０２１０】図１９は図３のアナログ－デジタル変換回路１における減算増幅回路１４ａの構成の第２の例を示す回路図である。

【０２１１】図１９の減算増幅回路１４ａは、演算増幅器１３０、コンデンサ１３９，１４０、容量値切り替え回路１４１，１４２およびスイッチ１３５～１４０を含む。

【０２１２】演算増幅器１３０の反転入力端子と反転出力端子との間にフィードバック容量としてコンデンサ１３９が接続され、非反転入力端子と非反転出力端子との間にフィードバック容量としてコンデンサ１４０が接続されている。また、演算増幅器１３０の反転入力端子に入力容量として容量値切り替え回路１４１が接続され、非反転入力端子に入力容量として容量値切り替え回路１４２が接続されている。

【０２１３】図３の演算増幅回路１１から出力される正側アナログ出力電圧Ｖｏ（＋）およびＤ／Ａコンバータ１０ｂから出力される差動正側出力電圧ＶＤＡ（＋）がそれぞれスイッチ１３５、１３６を介して容量値切り替え回路１４１に与えられる。また、演算増幅回路１１から出力される負側アナログ出力電圧Ｖｏ（－）およびＤ／Ａコンバータ１０ｂから出力される差動正側出力電圧ＶＤＡ（－）がそれぞれスイッチ１３７，１３８を介して容量値切り替え回路１４２に与えられる。演算増幅器１３０の反転入力端子、反転出力端子、非反転入力端子および非反転出力端子は、それぞれスイッチ１３９，１４０、１４１、１４２を介して接地されている。

【０２１４】図１９の減算増幅回路１４ａの動作は、図５の演算増幅回路１１ａの動作と同様である。演算増幅器１３０の反転出力端子および非反転出力端子からは次段の回路４へ与えられる正側アナログ入力電圧Ｖｉｎ（＋）および負側アナログ入力電圧Ｖｉｎ（－）が得られる。

【０２１５】ここで、容量値切り替え回路１４１，１４２の容量値を切り替えることにより、減算増幅回路１４ａの利得を切り替えることができる。

【０２１６】上記の実施の形態のスイッチＳａ、Ｓ１ａ、Ｓ２ａ，Ｓ２４，Ｓ２５，Ｓ２６、Ｓ２８、Ｓ２９、Ｓ３０，Ｓ３１は、例えばＭＯＳ（金属酸化物半導体）電界効果トランジスタにより形成される。

【０２１７】上記実施の形態では、切り替え手段の切り替え部としてスイッチＳａ、Ｓ１ａ、Ｓ２ａ，Ｓ２４，Ｓ２５，Ｓ２６、Ｓ２８、Ｓ２９，Ｓ３０，Ｓ３１を用いている。この場合には、製造時または使用時にスイッチＳａ，Ｓ１ａ、Ｓ２ａ、Ｓ２４，Ｓ２５，Ｓ２６，Ｓ２８、Ｓ２９、Ｓ３０，Ｓ３１をオンまたはオフに切り替えることができる。切り替え手段の切り替え部はスイッチに限定されない。例えば、切り替え部としてレーザにより溶断可能なヒューズを用いてもよく、切り替え部として最上層金属のパターニング用マスク切り替え部を用いてもよい。

【０２１８】図２０は切り替え部の他の例を示す回路図である。図２０の例では、図６の演算増幅回路１１ａのスイッチＳａの代わりにヒューズＦａを用いている。ヒューズＦａは、例えばポリシリコンからなり、レーザにより溶断可能である。製造時に、ヒューズＦａをレーザを用いて溶断するか否かにより演算増幅回路１１ａの利得を切り替えることができる。

【０２１９】図２１および図２２は切り替え部のさらに他の例を示す図であり、上部に平面図を示し、下部に断面図を示す。

【０２２０】容量形成部Ｃ５００において、下層金属ＬＭ１、ＬＭ２によりコンデンサの電極５０１，５０２が形成されている。また、下層金属ＬＭ１により電極５０７，５０８が形成されている。さらに、最上層金属ＵＭにより、所定間隔で電極５１２，５１３が形成されかつ所定間隔で電極５１４，５１５が形成されている。電極５０１はスルーホール５０３内の金属を介して電極５１２に接続され、電極５０２はスルーホール５０４内の金属を介して電極５１４に接続されている。また、電極５０７はスルーホール５０５内の金属を介して電極５１２に接続され、電極５０８はスルーホール５０６内の金属を介して電極５１５に接続されている。

【０２２１】例えば、５０７は図６の演算増幅器１１０の反転入力端子に接続され、電極５０８は図６の演算増幅器１１０の反転出力端子に接続される。

【０２２２】電極５０１、５０２により容量形成部Ｃ５００が形成され、電極５１２，５１３間および電極５１４，５１５間によりマスク切り替え部ＭＳＷがそれぞれ形成される。容量形成ブロックＣ５００は、例えば図６のコンデンサＣａに相当する。

【０２２３】製造時に、マスク切り替え部ＭＳＷ上に配置するマスクのパターンを変更することにより、電極５１２，５１３間および電極５１４，５１５間を接続状態および遮断状態に切り替えることができる。

【０２２４】図２１に示すように、電極５１２，５１３間および電極５１４，５１５間に最上層金属ＵＭにより金属層５１０，５１１が形成されるようなマスクを用いることにより、電極５１２，５１３間および電極５１

４，５１５間を接続することができる。

【０２２５】図２２に示すように、電極５１２，５１３間および電極５１４，５１５間に最上層金属層ＵＭにより金属層が形成されないようなマスクを用いることにより，電極５１２，５１３間および電極５１４，５１５間を遮断することができる。

【０２２６】図２１および図２２の例では、容量形成部Ｃ５００の両方の端子にマスク切り替え部をそれぞれ設けることにより，容量形成部Ｃ５００を演算増幅器から完全に切り離すことができる。

【０２２７】なお、本発明は、上記実施の形態に限定されず，アナログ－デジタル変換回路の任意の段の回路において、切り替え可能な利得を有する減算増幅回路、切り替え可能な利得を有する減算増幅回路、切り替え可能なフルスケールレンジを有するサブＡ／Ｄコンバータおよび切り替え可能なフルスケールレンジを有するＤ／Ａコンバータのうち少なくとも１つを用いてもよい。

【図面の簡単な説明】

【図１】本発明の第１の実施の形態におけるパイプライン型アナログ－デジタル変換回路の構成を示すブロック図である。

【図２】図１のアナログ－デジタル変換回路をそれぞれ差動ダブルエンド入力方式およびシングルエンド入力方式に切り替える場合の設定を示す図である。

【図３】本発明の第２の実施の形態におけるパイプライン型アナログ－デジタル変換回路の構成を示すブロック図である。

【図４】図１のアナログ－デジタル変換回路における演算増幅回路の構成の第１の例を示す回路図である。

【図５】図１のアナログ－デジタル変換回路における演算増幅回路の構成の第２の例を示す回路図である。

【図６】演算増幅回路の具体的な回路構成の第１の例を示す回路図である。

【図７】演算増幅回路の具体的な回路構成の第２の例を示す回路図である。

【図８】演算増幅回路の具体的な回路構成の第３の例を示す回路図である。

【図９】演算増幅回路の具体的な回路構成の第４の例を示す回路図である。

【図１０】演算増幅回路の具体的な回路構成の第５の例を示す回路図である。

【図１１】演算増幅回路の具体的な回路構成の第６の例を示す回路図である。

【図１２】図１のアナログ－デジタル変換回路におけるサブＡ／Ｄコンバータの構成の第１の例を示す回路図である。

【図１３】図１２のサブＡ／Ｄコンバータに用いられるコンパレータの構成を示す回路図である。

【図１４】図１のアナログ－デジタル変換回路におけるサブＡ／Ｄコンバータの構成の第２の例を示す回路図である。

【図１５】図１４のサブＡ／Ｄコンバータに用いられるコンパレータの構成を示す回路図である。

【図１６】図３のアナログ－デジタル変換回路における２段目の回路内のサブＡ／Ｄコンバータの回路図である。

【図１７】図３のアナログ－デジタル変換回路における２段目の回路内のＤ／Ａコンバータの回路図である。

【図１８】図３のアナログ－デジタル変換回路における減算増幅回路の構成の第１の例を示す回路図である。

【図１９】図３のアナログ－デジタル変換回路における減算増幅回路の構成の第２の例を示す回路図である。

【図２０】切り替え手段の切り替え部の他の例を示す回路図である。

【図２１】切り替え手段の切り替え部のさらに他の例を示す平面図および断面図である。

【図２２】切り替え手段の切り替え部のさらに他の例を示す平面図および断面図である。

【図２３】従来のアナログ－デジタル変換回路を示すブロック図である。

【図２４】図２３のアナログ－デジタル変換回路の減算増幅回路の構成を示す回路図およびその減算増幅回路の動作を説明するための図である。

【図２５】図２３のアナログ－デジタル変換回路において用いられるサブＡ／Ｄコンバータの構成を示す図である。

【図２６】差動ダブルエンド入力およびシングルエンド入力におけるアナログ－デジタル変換を説明するための図である。

【符号の説明】

１　アナログ－デジタル変換回路
３～６　１段目～４段目の回路
９，９ａ，９ｂ　サブＡ／Ｄコンバータ
１０，１０ｂ　Ｄ／Ａコンバータ
１１，１３，１３ａ　演算増幅回路
１２　減算回路
１４，１４ａ　減算増幅回路
ＶＲＴ，ＶＲＴ２，ＶＲＴ３　高電位側基準電圧
ＶＲＢ，ＶＲＢ２，ＶＲＢ３　低電位側基準電圧
ＶＲＴ１　中間基準電圧
Ｓａ，Ｓ１ａ，Ｓ１ｂ，Ｓ２４，Ｓ２５，Ｓ２６，Ｓ２６，Ｓ２８，Ｓ２９，Ｓ３０，Ｓ３１　スイッチ

４、５１５間を接続することができる。

【０２２５】図２２に示すように、電極５１２、５１３間および電極５１４、５１５間に最上層金属ＵＭにより金属層が形成されないようなマスクを用いることにより、電極５１２、５１３間および電極５１４、５１５間を遮断することができる。

【０２２６】図２１および図２２の例では、容量形成部Ｃ５００の両方の端子にマスク切り替え部をそれぞれ設けることにより、容量形成部Ｃ５００を演算増幅器から完全に切り離すことができる。

【０２２７】なお、本発明は、上記実施の形態に限定されず、アナログ－デジタル変換回路の任意の段の回路において、切り替え可能な利得を有する減算増幅回路、切り替え可能な利得を有する減算増幅回路、切り替え可能なフルスケールレンジを有するサブＡ／Ｄコンバータおよび切り替え可能なフルスケールレンジを有するＤ／Ａコンバータのうち少なくとも１つを用いてもよい。

【図面の簡単な説明】

【図１】本発明の第１の実施の形態におけるパイプライン型アナログ－デジタル変換回路の構成を示すブロック図である。

【図２】図１のアナログ－デジタル変換回路をそれぞれ差動ダブルエンド入力方式およびシングルエンド入力方式に切り替える場合の設定を示す図である。

【図３】本発明の第２の実施の形態におけるパイプライン型アナログ－デジタル変換回路の構成を示すブロック図である。

【図４】図１のアナログ－デジタル変換回路における演算増幅回路の構成の第１の例を示す回路図である。

【図５】図１のアナログ－デジタル変換回路における演算増幅回路の構成の第２の例を示す回路図である。

【図６】演算増幅回路の具体的な回路構成の第１の例を示す回路図である。

【図７】演算増幅回路の具体的な回路構成の第２の例を示す回路図である。

【図８】演算増幅回路の具体的な回路構成の第３の例を示す回路図である。

【図９】演算増幅回路の具体的な回路構成の第４の例を示す回路図である。

【図１０】演算増幅回路の具体的な回路構成の第５の例を示す回路図である。

【図１１】演算増幅回路の具体的な回路構成の第６の例を示す回路図である。

【図１２】図１のアナログ－デジタル変換回路におけるサブＡ／Ｄコンバータの構成の第１の例を示す回路図である。

【図１３】図１２のサブＡ／Ｄコンバータに用いられるコンパレータの構成を示す回路図である。

【図１４】図１のアナログ－デジタル変換回路におけるサブＡ／Ｄコンバータの構成の第２の例を示す回路図である。

【図１５】図１４のサブＡ／Ｄコンバータに用いられるコンパレータの構成を示す回路図である。

【図１６】図３のアナログ－デジタル変換回路における２段目の回路内のサブＡ／Ｄコンバータの回路図である。

【図１７】図３のアナログ－デジタル変換回路における２段目の回路内のＤ／Ａコンバータの回路図である。

【図１８】図３のアナログ－デジタル変換回路における減算増幅回路の構成の第１の例を示す回路図である。

【図１９】図３のアナログ－デジタル変換回路における減算増幅回路の構成の第２の例を示す回路図である。

【図２０】切り替え手段の切り替え部の他の例を示す回路図である。

【図２１】切り替え手段の切り替え部のさらに他の例を示す平面図および断面図である。

【図２２】切り替え手段の切り替え部のさらに他の例を示す平面図および断面図である。

【図２３】従来のアナログ－デジタル変換回路を示すブロック図である。

【図２４】図２３のアナログ－デジタル変換回路の減算増幅回路の構成を示す回路図およびその減算増幅回路の動作を説明するための図である。

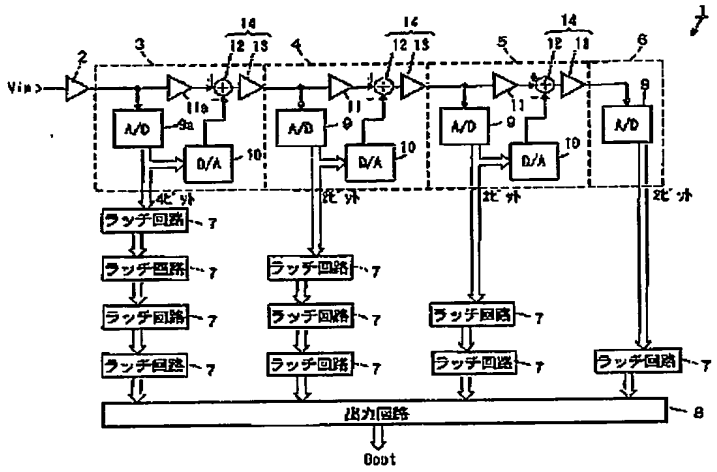
【図２５】図２３のアナログ－デジタル変換回路において用いられるサブＡ／Ｄコンバータの構成を示す図である。

【図２６】差動ダブルエンド入力およびシングルエンド入力におけるアナログ－デジタル変換を説明するための図である。

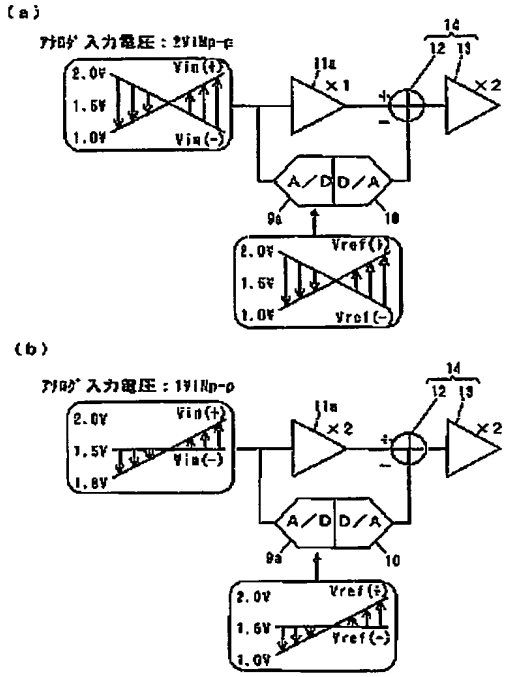
【符号の説明】

１　アナログ－デジタル変換回路
３～６　１段目～４段目の回路
９、９ａ，９ｂ　サブＡ／Ｄコンバータ
１０、１０ｂ　Ｄ／Ａコンバータ
１１、１３、１３ａ　演算増幅回路
１２　減算回路
１４、１４ａ　減算増幅回路
ＶＲＴ，ＶＲＴ２，ＶＲＴ３　高電位側基準電圧
ＶＲＢ，ＶＲＢ２，ＶＲＢ３　低電位側基準電圧
ＶＲＴ１　中間基準電圧
Ｓａ、Ｓ１ａ、Ｓ１ｂ，Ｓ２４，Ｓ２５，Ｓ２６、Ｓ２６、Ｓ２８，Ｓ２９，Ｓ３０，Ｓ３１　スイッチ

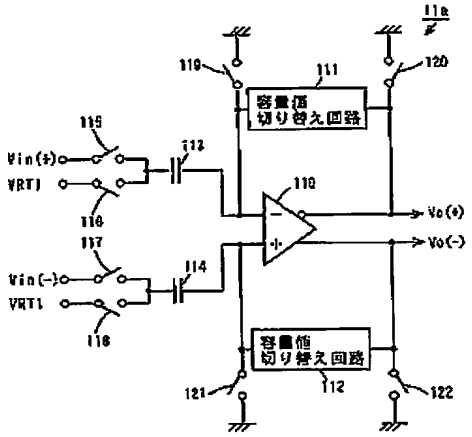
【図１】


Vin
A/D
D/A
4ビット
ラッチ回路
出力回路
Dout

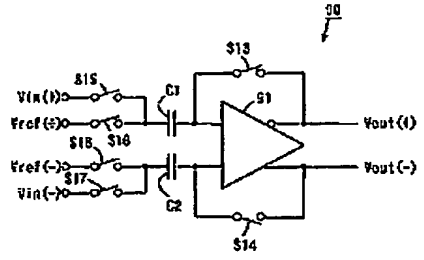
【図２】


(a)
アナログ入力電圧：2VppーP
2.0V
1.5V
1.0V
Vin(+)
Vin(-)
×1
×2
A/D D/A
Vref(+)
Vref(-)
(b)
アナログ入力電圧：1VppーP

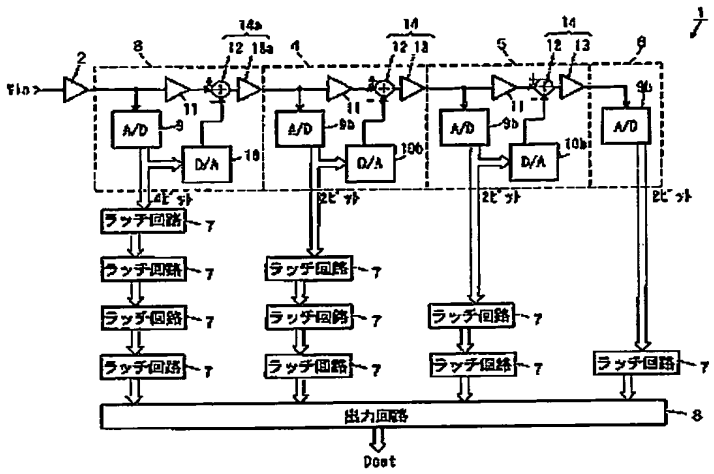
【図４】


容量値切り替え回路
Vin(+)
VRT1
Vin(-)
Vo(+)
Vo(-)

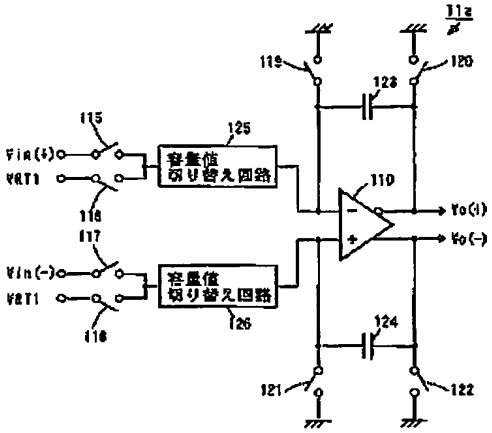
【図１３】


Vin(+)
Vref(+)
Vref(-)
Vin(-)
Vout(+)
Vout(-)

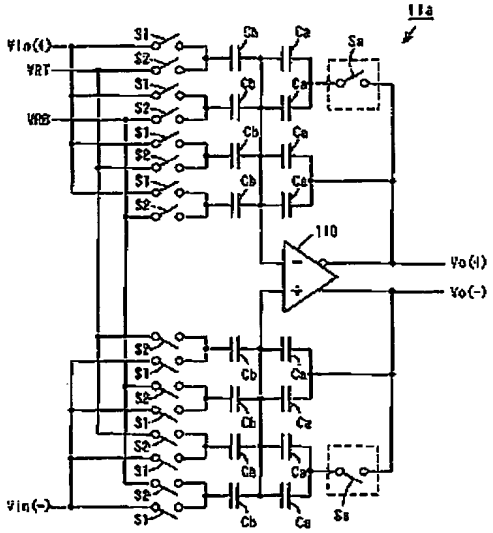
【図３】



【図５】



【図６】



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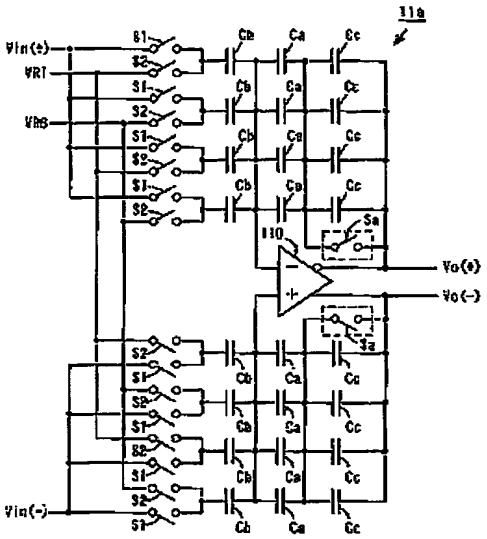
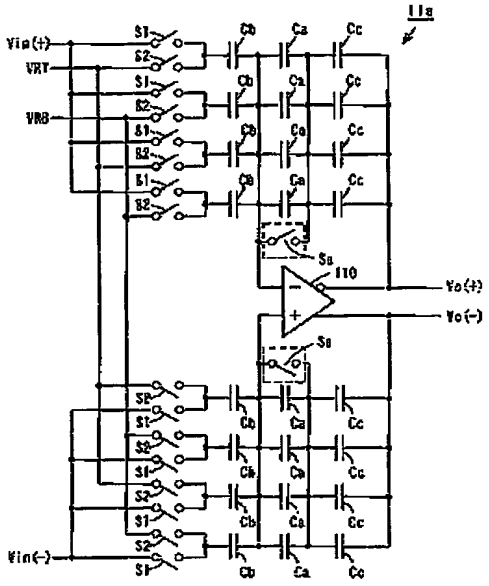
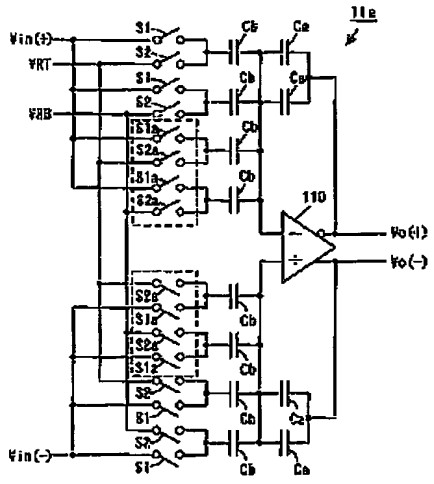

11a
Vin(+)
VRT
VRB
Vin(-)
S1
S2
Cb
Ca
Cc
Sa
110
Vo(+)
Vo(-)

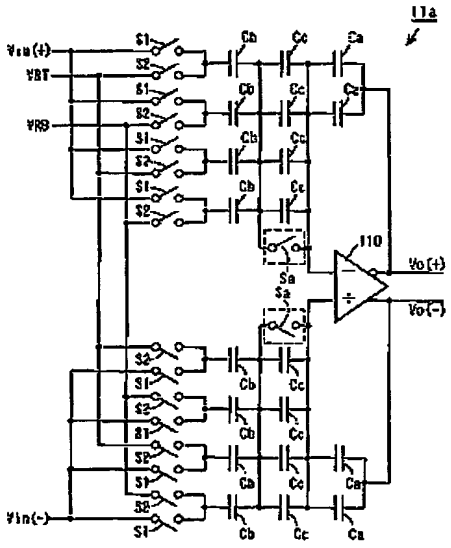
【図８】


11a
Vin(+)
VRT
VRB
Vin(-)
S1
S2
Cb
Ca
Cc
Sa
110
Vo(+)
Vo(-)

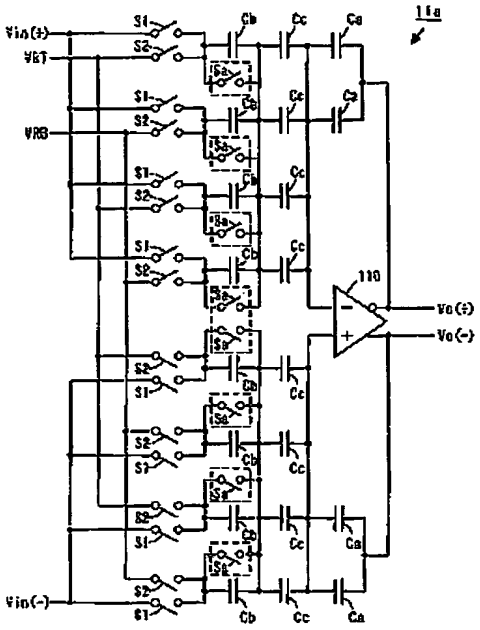
【図９】


11a
Vin(+)
VRT
VRB
Vin(-)
S1
S2
Cb
Ca
Cc
110
Vo(+)
Vo(-)

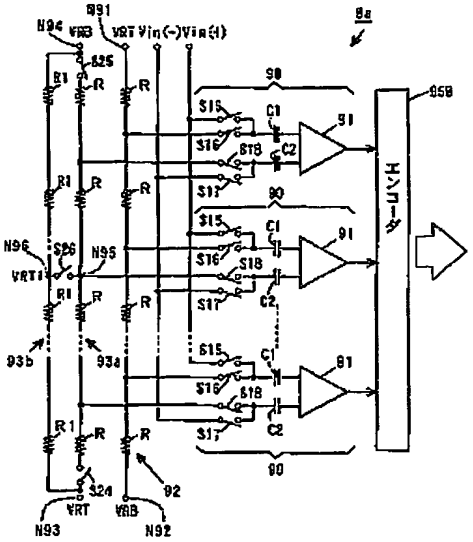
【図１０】


11a
Vin(+)
VRT
VRB
Vin(-)
S1
S2
Cb
Ca
Cc
Sa
110
Vo(+)
Vo(-)

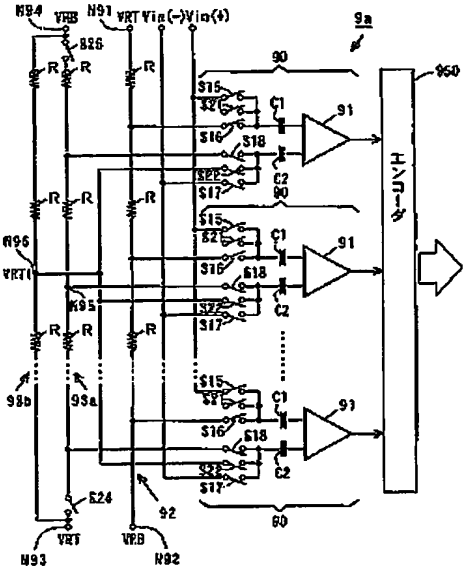
【図１１】



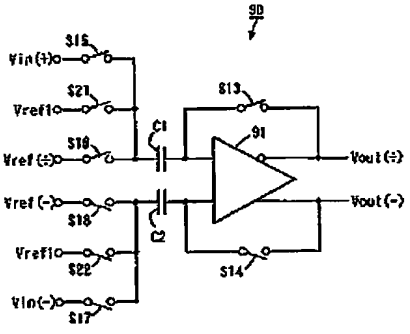
【図１２】



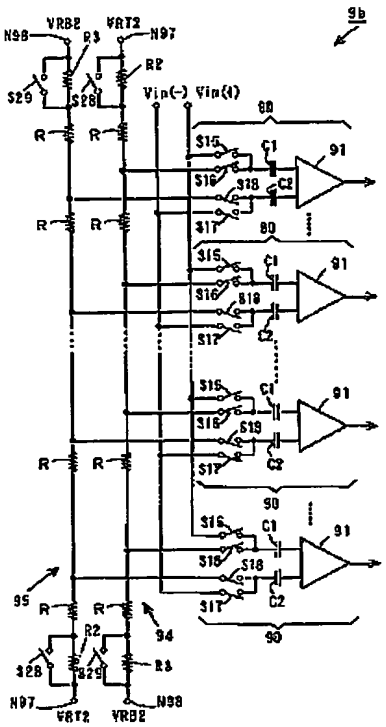
【図１４】



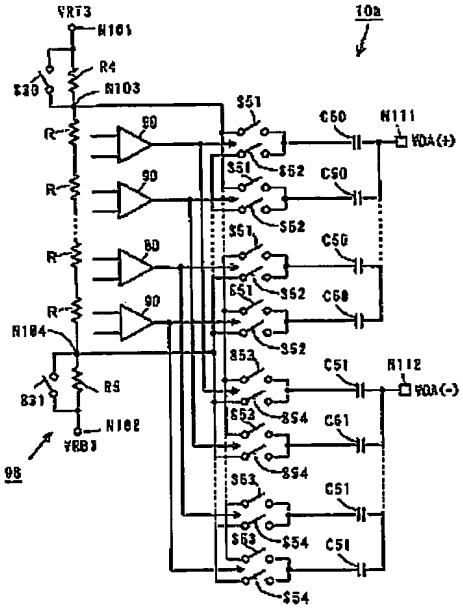
【図１５】



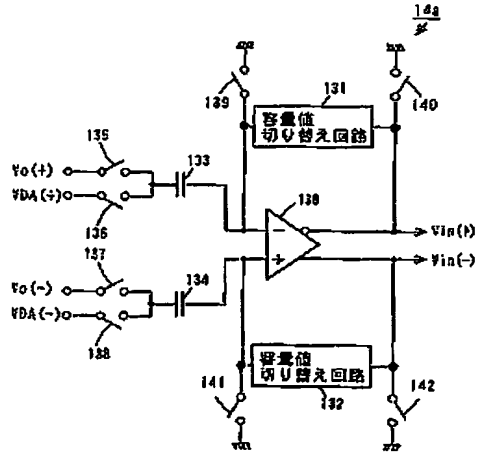
【図１６】



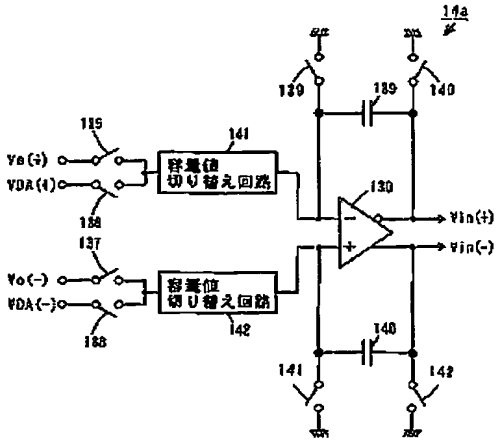
【図１７】



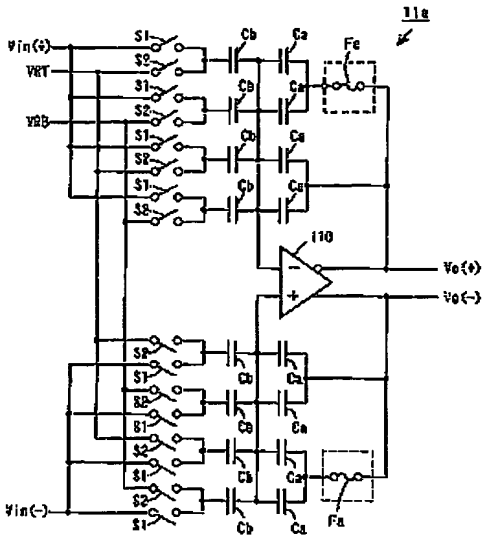
【図１８】



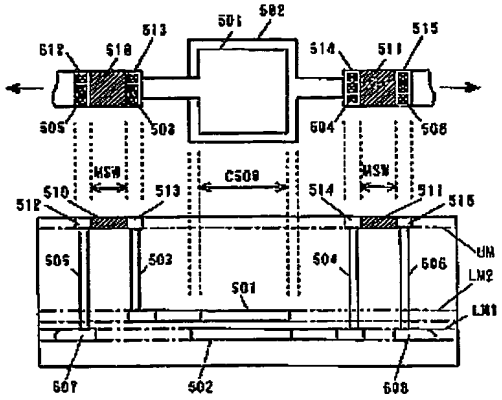
【図１９】



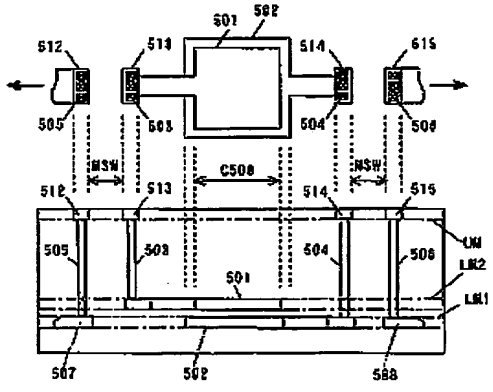
【図20】



【図21】

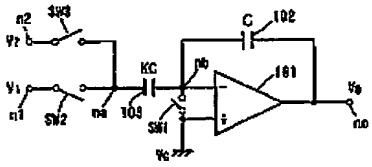


【図22】

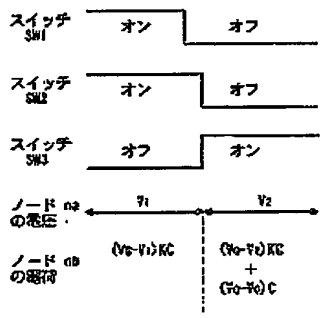


【図24】

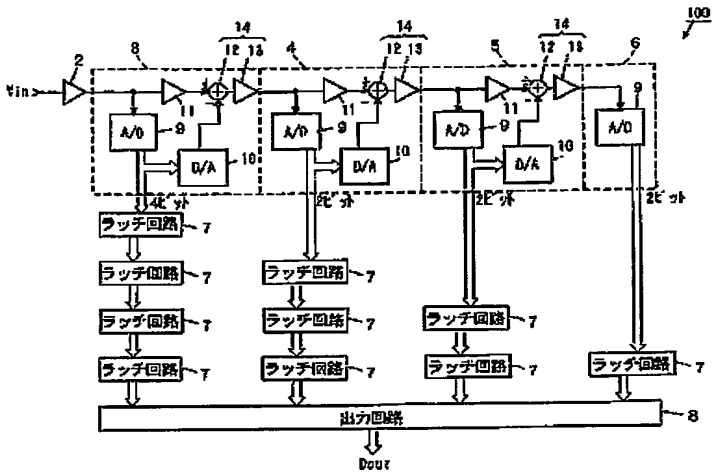
(a)



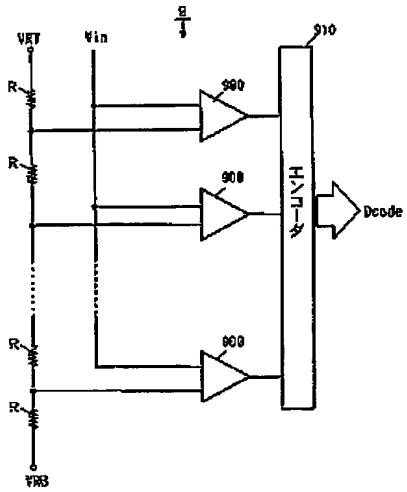
(b)



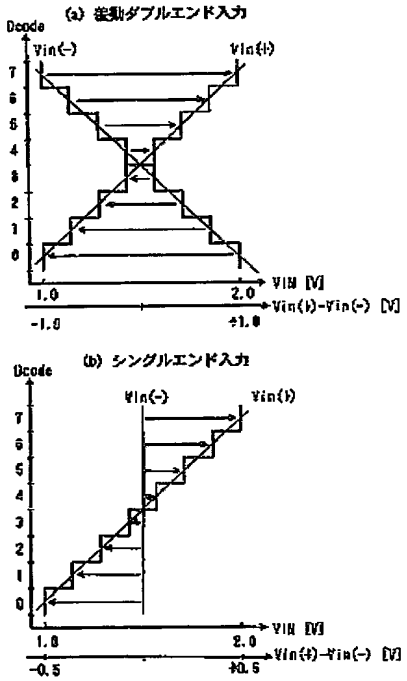
【図２３】


100
Vin
A/D
D/A
ラッチ回路
出力回路
Dout

【図２５】


VRT
Vin
VRB
910
900
908
909
エンコーダ
Dcode

【図２６】


(a) 差動ダブルエンド入力
Dcode
Vin(-)
Vin(+)
VIN [V]
Vin(+)-Vin(-) [V]
(b) シングルエンド入力

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Ｆターム(参考)　5J022 AA15 AB01 AC02 BA01 BA05 CA10 CB06 CC01 CD03 CE01 CE08 CF02 CF07